❖ Introduction

Digital integrated circuits are produced using several different circuit configurations and production technologies. Each such approach is called a specific logic family. The idea is that different logic functions, when fabricated in the form of an IC with the same approach, or in other words belonging to the same logic family, will have identical electrical characteristics. These characteristics include supply voltage range, speed of response, power dissipation, input and output logic levels, current sourcing and sinking capability, fan-out, noise margin, etc. The entire range of digital ICs is fabricated using either bipolar devices or metal oxide semiconductor (MOS) devices or a combination of the two. Different logic families falling in the first category are called bipolar families, and these include Diode Logic (DL), Resistor Transistor Logic (RTL), diode transistor logic (DTL), Transistor Transistor logic (TTL), Emitter Coupled Logic (ECL), also known as Current Mode Logic (CML), and Integrated Injection Logic (I^2L). The logic families that use MOS devices as their basis are known as MOS families, and the prominent members belonging to this category are the PMOS family (using P-channel MOSFETs), the NMOS family (using N-channel MOSFETs) and the CMOS family (using both N- and P-channel devices). The Bi-MOS logic family uses both bipolar and MOS devices. Of all the logic families listed above, the first three, that is, diode logic (DL), resistor transistor logic (RTL) and diode transistor logic (DTL), are of historical importance only. Diode logic used diodes and resistors and in fact was never implemented in integrated circuits. The RTL family used

resistors and bipolar transistors, while the DTL family used resistors, diodes and bipolar transistors. Both RTL and DTL suffered from large propagation delay owing to the need for the transistor base charge to leak out if the transistor were to switch from conducting to no conducting state. Figure 1 shows the simplified schematics of a two-input AND gate using DL [Fig. 1(a)], a two-input NOR gate using RTL [Fig.1(b)] and a two-input NAND gate using DTL [Fig.1(c)].

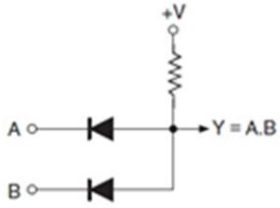


Fig. 1(a)

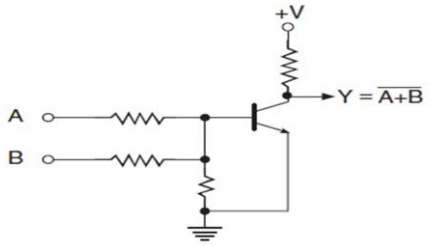


Fig. 1(b)

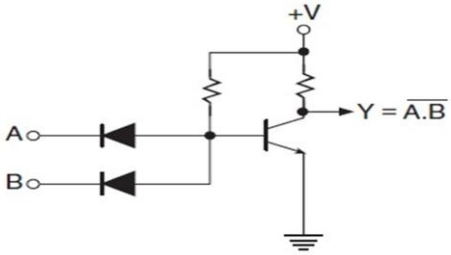


Fig. 1(c)

❖ ***Characteristic Parameters***

The parameters that used to characterize different logic families are listed:

1- HIGH-level input current, I_{IH}. This is the current flowing into (taken as positive) or out of (taken as negative) an input when a HIGH-level input voltage equal to the minimum HIGH-level output voltage specified for the family is applied. In the case of bipolar logic families such as TTL, the circuit design is such that this current flows into the input pin and is therefore specified as positive. In the case of CMOS logic families, it could be either positive or negative, and only an absolute value is specified in this case.

2- LOW-level input current, I_{IL}. The LOW-level input current is the maximum current flowing into (taken as positive) or out of (taken as negative) the input of a logic function when the voltage applied at the input equals the maximum LOW-level output voltage specified for the family. In the case of bipolar logic families such as TTL, the circuit design is such that this current flows out of the input pin and is therefore specified as negative. In the case of CMOS logic families, it could be either positive or negative. In this case, only an absolute value is specified. HIGH-level and LOW-level input current or loading are also sometimes defined in terms

of unit load (UL). For devices of the TTL family, $1\ UL\ (HIGH) = 40A\ and\ 1\ UL\ (LOW) = 1.6\ mA$.

3- HIGH-level output current, I_{OH}. This is the maximum current flowing out of an output. It is normally shown as a negative number. The magnitude of I_{OH} determines the number of inputs the logic function can drive when its output is in the logic HIGH state. For example, for the standard TTL family, the minimum guaranteed I_{OH} is $-400\ \mu A$, which can drive 10 standard TTL inputs with each requiring $40\ \mu A$ in the HIGH state, as shown in Fig.2(a).

4- LOW-level output current, I_{OL}. This is the maximum current flowing into the output pin of a logic function when the input conditions are such that the output is in the logic LOW state. The magnitude of I_{OL} determines the number of inputs the logic function can drive when its output is in the logic LOW state. For example, for the standard TTL family, the minimum guaranteed I_{OL} is $16\ mA$, which can drive 10 standard TTL inputs with each requiring $1.6mA$ in the LOW state, as shown in Fig.2(b).

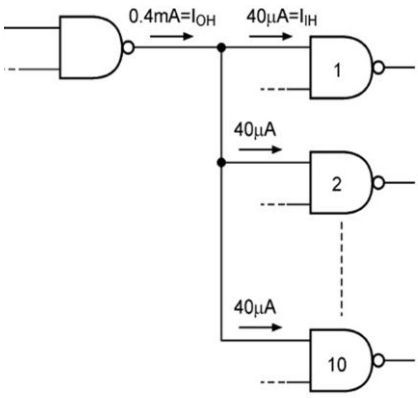


Fig. 2(a)

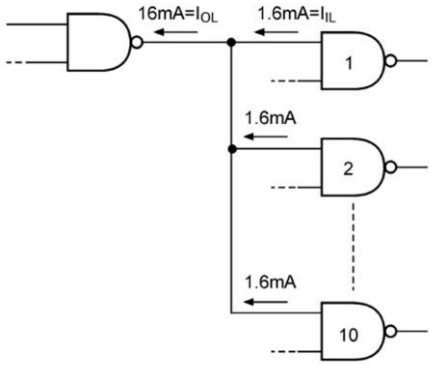


Fig. 2(b)

5- HIGH-level off-state (high-impedance state) output current, I_{OZH}. This is the current flowing into an output of a tristate logic function with the enable input chosen so as to establish a high-impedance state and a logic HIGH voltage level applied at the output. The input conditions are chosen so as to produce logic LOW if the device is enabled.

6- LOW-level off-state (high-impedance state) output current, I_{OZL}. This is the current flowing into an output of a tristate logic function with the enable input chosen so as to establish a high-impedance

state and a logic LOW voltage level applied at the output. The input conditions are chosen so as to produce logic HIGH if the device is enabled.

7- HIGH-level input voltage, V_{IH}. This is the minimum voltage level that needs to be applied at the input to be recognized as a legal HIGH level for the specified family. For the standard TTL family, $a\ 2\ V$ input voltage is a legal HIGH logic state. 120 Digital Electronics LOW-level input voltage, V_{IL}. This is the maximum voltage level applied at the input that is recognized as a legal LOW level for the specified family. For the standard TTL family, an input voltage of $0.8\ V$ is a legal LOW logic state.

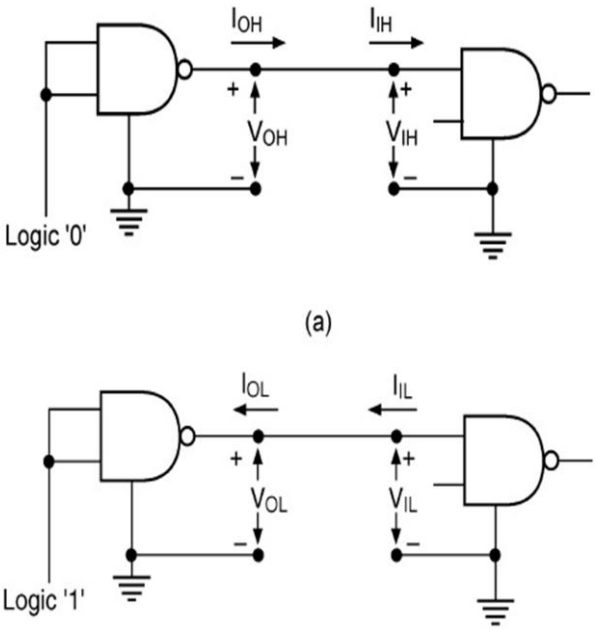
8- HIGH-level output voltage, V_{OH}. This is the minimum voltage on the output pin of a logic function when the input conditions establish logic HIGH at the output for the specified family. In the case of the standard TTL family of devices, the HIGH level output voltage can be as low as $2.4V$ and still be treated as a legal HIGH logic state. It may be mentioned here that, for a given logic family, the V_{OH} specification is always greater than the V_{IH} specification to ensure output-to-input compatibility when the output of one device feeds the input of another.

9- LOW-level output voltage, V_{OL}. This is the maximum voltage on the output pin of a logic function when the input conditions establish logic LOW at the output for the specified family. In the case of the standard TTL family of devices, the LOW-level output voltage can be as high as $0.4V$ and still be treated as a legal LOW logic state. It may be mentioned here that, for a given logic family, the VOL specification is always smaller than the V_{IL} specification to ensure output-to-input compatibility when the output of one device feeds the input of another.

The different input/output current and voltage parameters are shown in Fig.3, with HIGH-level current and voltage parameters in Fig.3(a) and LOW-level current and voltage parameters in Fig.3(b).

It may be mentioned here that the direction of the LOW-level input and output currents shown in Fig.3(b) is applicable to logic families with current-sinking action such as TTL.

10- Supply current, I_{CC}. The supply current when the output is HIGH, LOW and in the high-impedance state is respectively designated as I_{CCH}, I_{CCL} and I_{CCZ}.



(a)

(b)

Fig.3

11- Rise time, t_r. This is the time that elapses between 10 and 90 % of the final signal level when the signal is making a transition from logic LOW to logic HIGH.

12- Fall time, t_f . This is the time that elapses between 90 and 10 % of the signal level when it is making HIGH to LOW transition.

13- Propagation delay t_p. The propagation delay is the time delay between the occurrence of change in the logical level at the input and before it is reflected at the output. It is the time delay between the specified voltage points on the input and output waveforms. Propagation delays are separately defined for LOW-to-HIGH and HIGH-to-LOW transitions at the output. Propagation delay tpLH. This is the time delay between specified voltage points on the input and output waveforms with the output changing from LOW to HIGH.

14- Propagation delay t_p HL. This is the time delay between specified voltage points on the input and output waveforms with the output changing from HIGH to LOW. Figure 4 shows the two types of propagation delay parameter.

15- Disable time from the HIGH state, t_p HZ. Defined for a tristate device, this is the time delay between specified voltage points on the input and output waveforms with the tristate output changing from the logic HIGH level to the high-impedance state.

16- Disable time from the LOW state, t_p LZ. Defined for a tristate device, this is the time delay between specified voltage points on the input and output waveforms with the tristate output changing from the logic LOW level to the high-impedance state.

17- Enable time from the HIGH state, t_p ZH. Defined for a tristate device, this is the time delay between specified voltage points on the input and output waveforms with the tristate output changing from the high-impedance state to the logic HIGH level.

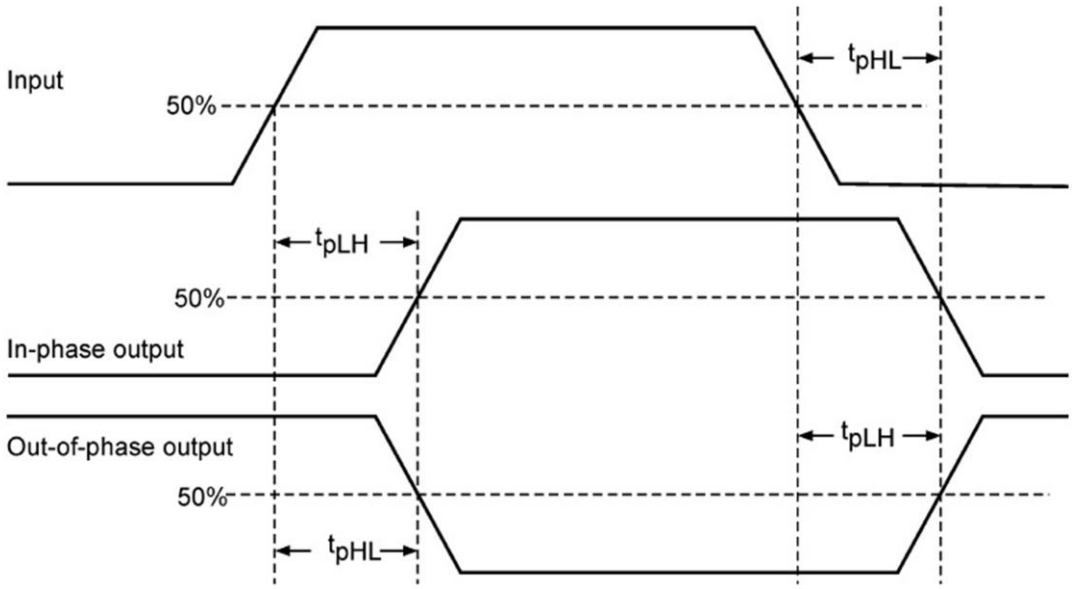


Fig.4

18- **Enable time from the LOW state, t_p ZL.** Defined for a tristate device, this is the time delay between specified voltage points on the input and output waveforms with the tristate output changing from the high-impedance state to the logic LOW level.

19- **Maximum clock frequency, $fmax$.** This is the maximum frequency at which the clock input of a flip-flop can be driven through its required sequence while maintaining stable transitions of logic level at the output in accordance with the input conditions and the product specification. It is also referred to as the maximum toggle rate for a flip-flop or counter device.

20- **Power dissipation.** The power dissipation parameter for a logic family is specified in terms of power consumption per gate

and is the product of supply voltage V_{CC} and supply current I_{CC}. The supply current is taken as the average of the HIGH-level supply current I_{CCH} and the LOW-level supply current I_{CCL}.

21- **Speed–power product.** The speed of a logic circuit can be increased, that is, the propagation delay can be reduced, at the expense of power dissipation. We will recall that, when a bipolar transistor switches between cut-off and saturation, it dissipates the least power but has a large associated switching time delay. On the other hand, when the transistor is operated in the active region, power dissipation goes up while the switching time decreases drastically. It is always desirable to have in a logic family low values for both propagation delay and power dissipation parameters.

22- **Fan-out.** The fan-out is the number of inputs of a logic function that can be driven from a single output without causing any false output.

23- **Noise margin.** This is a quantitative measure of noise immunity offered by the logic family. Figure (5) shows the generalized case of legal HIGH and LOW voltage levels for output [Fig.5(a)] and input [Fig.5(b)]. As we can see from the two diagrams, there is a disallowed range of output voltage levels from VOL(max.) to VOH(min.) and an indeterminate range of input voltage levels from VIL(max.) to VIH(min.). Since VIL(max.) is greater than VOL(max.), the LOW output state can therefore tolerate a positive voltage spike equal to VIL(max.) − VOL(max.) and still be a legal LOW input. Similarly, VOH(min.) is greater than VIH (min.), and the HIGH output state can tolerate a negative voltage spike equal to VOH(min.) – VIH (min.) and still be a legal HIGH input. Here, VIL(max.) − VOL(max.) and VOH(min.) − VIH (min.) are respectively known as the LOW-level and HIGH-level noise margin. Let us illustrate it further with the help of data for the standard TTL family. The minimum legal HIGH output voltage level in the case of the standard TTL is 2.4 V. Also, the minimum legal HIGH input voltage level for this family is 2 V. This implies that, when the output of one device feeds the input of another, there is an available margin of 0.4 V. That is, any negative voltage spikes of amplitude.

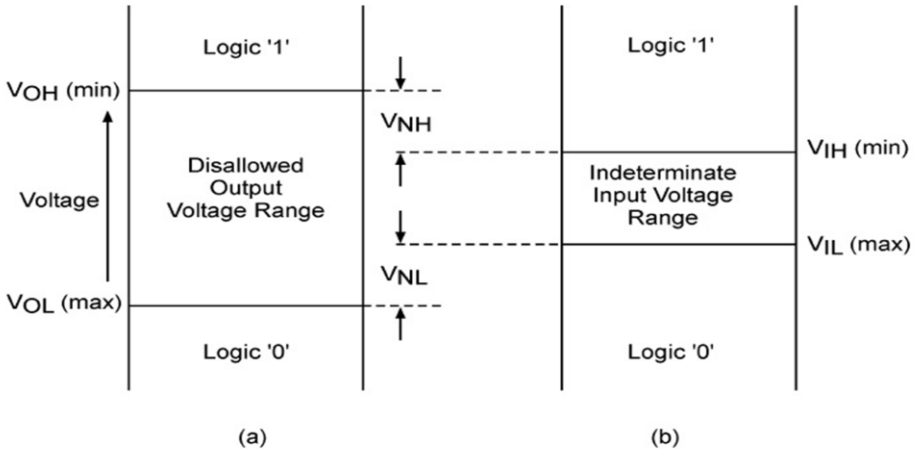


Fig.5

less than or equal to 0.4V on the signal line do not cause any spurious transitions. Similarly, when the output is in the logic LOW state, the maximum legal LOW output voltage level in the case of the standard TTL is 0.4 V. Also, the maximum legal LOW input voltage level for this family is 0.8 V. This implies that, when the output of one device feeds the input of another, there is again an available margin of 0.4 V. That is, any positive voltage spikes of amplitude less than or equal to 0.4V on the signal line do not cause any spurious transitions. This leads to the standard TTL family offering a noise margin of 0.4 V. To generalize, the noise margin offered by a logic family, as outlined earlier, can be computed from the HIGH-state noise margin, VNH = VOH(min.)−VIH(min.), and the LOW-state noise margin, VNL = VIL(max.) − VOL(max.).

❖ ***Diode Logic(DL)***

Diode Logic suffers from voltage degradation from one stage to the next, DL only permits the OR and AND functions, and DL is used extensively but not in integrated circuits.

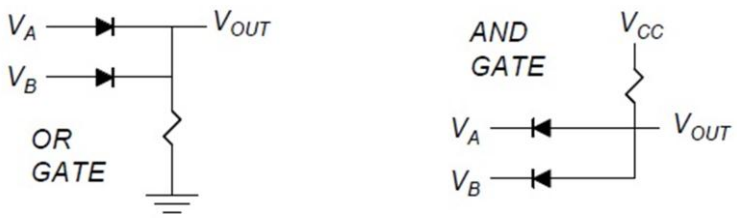


Fig.6

❖ Level-Shifted Diode Logic

With either input at $0V, Vx = 0.7V$, DL is just cut off, and $V_{OUT} = 0V$. With both inputs at $1V$, $V_X = 1.7V$ and $V_{OUT} = 1V$. With $V_A = V_B = 5V$, both input diodes are cut off. Then

$V_{out} = R_L(\frac{V_{cc}-0.7}{R_H+R_L})$

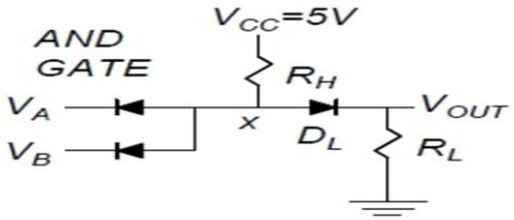


Fig.7

Level shifting eliminates the voltage degradation from the input to the output. However, the logic swing falls short of rail-to-rail, and the inverting function still is not available without using a transistor.

❖ Diode-Transistor Logic (DTL)

If any input goes high, the transistor saturates and V_{out} goes low, if all inputs are low, the transistor cuts off and V_{out} goes high, this is a NOR gate.

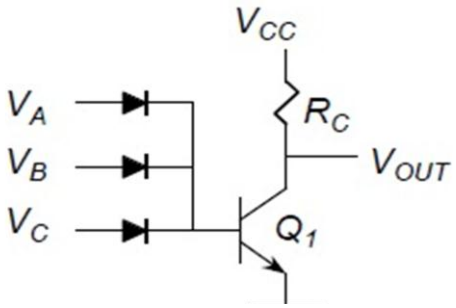


Fig.8

The NAND gate is given in figure (9). If all inputs are high, the transistor saturates and V_{out} goes low, if any input goes low, the base current is diverted out through the input diode. The transistor cuts off and V_{out} goes high.

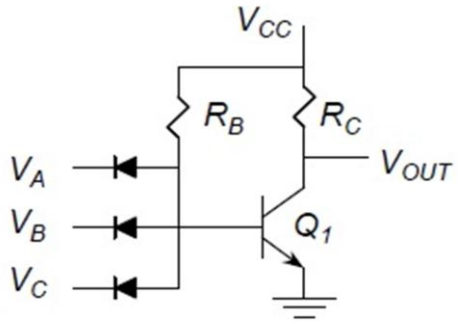


Fig.9

Ex_1/ The data sheet of a quad two-input NAND gate specifies the following parameters: $I_{OH}(max.) = 0.4\,mA, V_{OH}(min.) = 2.7\,V$, V_{IH} $(\ min.) = 2V, VIL(max.) = 0.8\,V, VOL(max.) = 0.4\,V, IOL(max.) = 8\,mA, I_{IL}(max.) = 0.4\,mA, IIH\ (max.) = 20\_A, ICCH(max.) = 1.6\,mA,\ I_{CCL}(max.) = 4.4\,mA, tpLH\ = tpHL\ = 15\,ns$ and a supply voltage range of $5\,V$. Determine (a) the average power dissipation of a single NAND gate, (b) the maximum average propagation delay of a single gate, (c) the HIGH-state noise margin and (d) the LOW-state noise margin

Sol:

(a) The average supply current $= (ICCH\ + ICCL\_/2 = (1.6\ + 4.4)/2 = 3\,mA.$

The supply voltage $VCC\ = 5V.$

Therefore, the power dissipation for all four gates in the

$IC = 5\ \times\ 3 = 15\,mW.$

The average power dissipation per gate $= 15/4 = 3.75\,mW.$

(b) The propagation delay $= 15\,ns.$

(c) The HIGH-state noise margin $= VOH(min.)$ – $VIH(min.)$ $= 2.7\ -\ 2 = 0.7\,V.$

(d) The LOW-state noise margin $= VIL(max.)\ -\ VOL(max.)$ $= 0.8\ -\ 0.4 = 0.4\,V.$

Ex_2/ Refer to example1 How many NAND gate inputs can be driven from the output of a NAND gate of this type?

Solution

- $HIGH - state\ fan - out = \frac{I_{OH}}{I_{IH}}$

=400/20 = 20.

- $The\ LOW - state\ fan - out = \frac{I_{OL}}{I_{IL}}$

$= 8/0.4 = 20.$

• Therefore, the number of inputs that can be driven from a single output=20.

Ex_3/ Determine the fan-out of IC 74LS04, given the following data: input loading factor (HIGH state)=0.5 UL, input loading factor (LOW state)=0.25 UL, output loading factor (HIGH state)=10 UL, output loading factor (LOW state)=5 UL, where UL is the unit load.

Solution

• The HIGH-state fan-out can be computed from: fan-out=output loading factor (HIGH)/input loading factor $(HIGH) = 10\ UL/0.5\ UL = 20$.

• The LOW-state fan-out can be computed from: fan-out = output loading factor (LOW)/input loading factor $(LOW) = 5\ UL/0.25\ UL = 20$.

• Since the fan-out in the two cases turns out to be the same, it follows that the $fan - out = 20$.

Ex_4/ A certain TTL gate has $I_{IH} = 20\ \_A,\ I_{IL} = 0.1\ mA, I_{OH} = 0.4\ mA$ and $I_{OL} = 4\ mA$. Determine the input and output loading in the HIGH and LOW states in terms of UL.

Solution

• $1\ UL\ (LOW\ state) = 1.6\ mA\ and\ 1\ UL\ (HIGH\ state) = 40\ \_A$.

• The input loading factor (HIGH state) $= 20\ \_A = 20/40 = 0.5\ UL$.

• The input loading factor (LOW state) $= 0.1mA = 0.1/1.6 = 1/16\ UL$

• The output loading factor (HIGH state) $= 0.4mA = 0.4/0.04 = 10\ UL$.

• The output loading factor (LOW state) $= 4mA = 4/1.6 = 2.5\ UL$.

❖ ***Transistor Transistor Logic (TTL)***

It is a logic family implemented with bipolar process technology that combines or integrates NPN transistors, PN junction diodes and diffused resistors in a single monolithic structure to get the desired logic function.

1- NAND Gate

The NAND gate is the basic building block of this logic family. Different subfamilies in this logic family, as outlined earlier, include standard TTL, low-power TTL, high-power TTL, low-power Schottky TTL, Schottky TTL, advanced low-power Schottky TTL, advanced Schottky TTL and fast TTL. Figure 10 shows the internal schematic of a standard TTL NAND gate. It is one of the four circuits of 5400/7400, which is a quad two-input NAND gate. The circuit operation is illustrated as:

When both the inputs are in the logic HIGH state as specified by the TTL family ($VIH = 2\ V$ minimum), the current flows through the base-

collector PN junction diode of transistor Q1 into the base of transistor Q2. Transistor Q2 is turned ON to saturation, with the result that transistor Q3 is switched OFF and transistor Q4 is switched ON. This produces a logic LOW at the output, with VOL being 0.4 V maximum when it is sinking a current of 16 mA from external loads represented by inputs of logic functions being driven by the output. The current-sinking action is shown in Fig. 5.11(a). Transistor Q4 is also referred to as the current-sinking or pull-down transistor, for obvious reasons. Diode D1 is used to prevent transistor Q3 from conducting even a small amount of current when the output is LOW. When the output is LOW, Q4 is in saturation and Q3 will conduct slightly in the absence of D1. Also, the input current IIH in the HIGH state is nothing but the reverse-biased junction diode leakage current and is typically 40 _A. When either of the two inputs or both inputs are in the logic LOW state, the base-emitter region of Q1 conducts current, driving Q2 to cut-off in the process. When Q2 is in the cut-off state, Q3 is driven to conduction and Q4 to cut-off. This produces a logic HIGH output with VOH(min.)=2.4 V guaranteed for minimum supply voltage VCC and a source current of 400 _A. The current-sourcing action is shown in Fig. 5.11(b). Transistor Q3 is also referred to as the current-sourcing or pull-up transistor. Also, the LOW-level input current IIL, given by (VCC −VBE1_/R1, is 1.6 mA (max.) for maximum VCC.

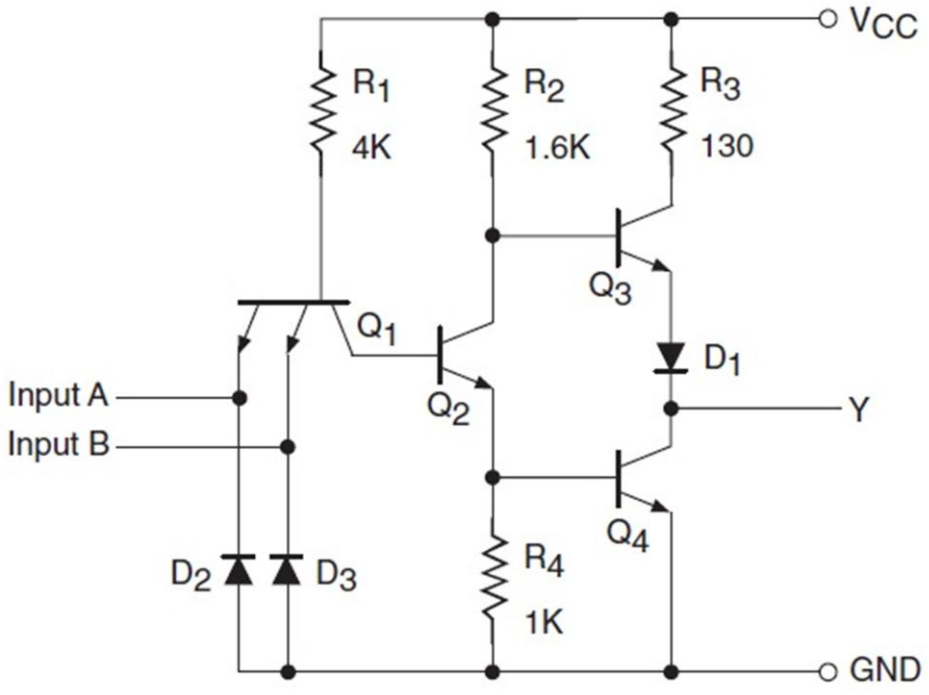


Fig. 10

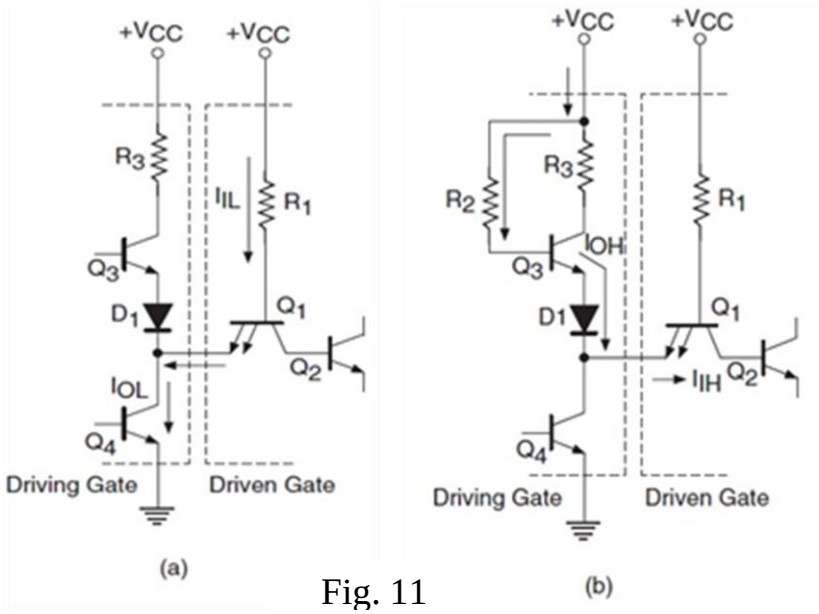


Fig. 11

The characteristic parameters and features of the standard TTL family of devices include the following: $VIL = 0.8\,V$; $VIH = 2V$; $IIH = 40\,A$; $IIL = 1.6\,mA$; $VOH = 2.4\,V$; $VOL = 0.4\,V$; $IOH = 400\_A$; $IOL = 16\,mA$; $VCC = 4.75–5.25V$ $(74-series)$ and $4.5–5.5V$ $(54-series)$; propagation delay (for a load resistance of 400Ω, a load capacitance of $15\,pF$ and an ambient temperature of $25^{\circ}\ C) = 22\,ns$ (max.) for LOW-to-HIGH transition at the output and 15 ns (max.) for HIGH to- LOW output transition; worst-case noise margin $= 0.4\,V$; $fan-out = 10$; ICCH (for all four gates) $= 8\,mA$; ICCL (for all four gates) $= 22\,mA$; operating temperature range $= 0–70\ ^{\circ}\ C$ $(74-\text{series})$ and $-55\ to\ +125\ ^{\circ}\ C$ $(54-\text{series})$; speed–power product $= 100\,pJ$; maximum flip-flop toggle frequency$= 35\,MHz$.

2- NOT Gate

Figure 11 shows the internal schematic of a NOT gate (inverter) in the standard TTL family. The schematic shown is that of one of the six inverters in a hex inverter (type 7404/5404). The internal schematic is just the same as that of the NAND gate except that the input transistor is a normal single emitter NPN transistor instead of a multi-emitter one.

3- NOR Gate

Figure 12 shows the internal schematic of a NOR gate in the standard TTL family. The schematic shown is that of one of the four NOR gates in a quad two-input NOR gate (type 7402/5402). On the

input side there are two separate transistors instead of the multi-emitter transistor of the NAND gate. The inputs are fed to the emitters of the two transistors, the collectors of which again feed the bases of the two transistors with their collector and emitter terminals tied together. The resistance values used are the same as those used in the case of the NAND gate. The output stage is also the same totem-pole output stage. The circuit is self-explanatory. The only input condition for which transistors Q3 and Q4 remain in cut-off, thus driving Q6 to cut-off and Q5 to conduction, is the one when both the inputs are in the logic LOW state. The output in such a case is logic HIGH. For all other input conditions, either Q3 or Q4 will conduct, driving Q6 to saturation and Q5 to cut-off, producing a logic LOW at the output.

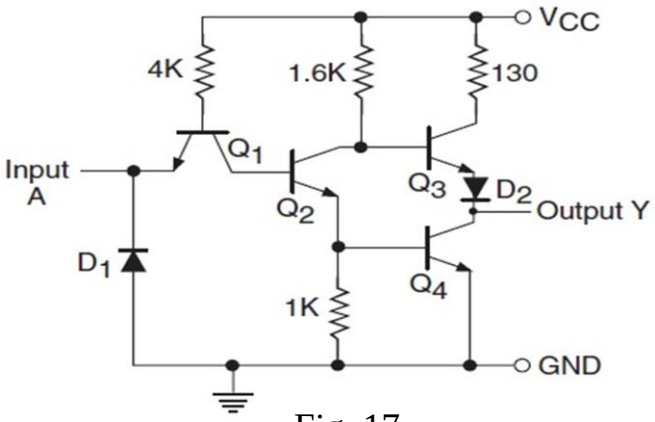


Fig. 17

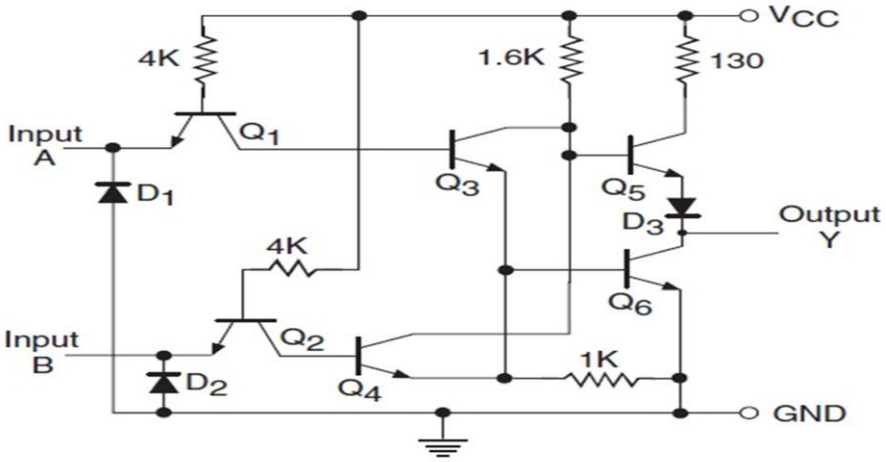


Fig. 18

4- AND Gate

Figure 19 shows the internal schematic of an AND gate in the standard TTL family. The schematic shown is that of one of the four AND gates in a quad two-input AND gate (type 7408/5408). In order

to explain how this schematic arrangement behaves as an AND gate, we will begin by investigating the input condition that would lead to a HIGH output. A HIGH output implies Q6 to be in cut-off and Q5 to be in conduction. This can happen only when Q4 is in cut-off. Transistor Q4 can be in the cut-off state only when both Q2 and Q3 are in conduction. This is possible only when both inputs are in the logic HIGH state. Let us now see what happens when either of the two inputs is driven to the LOW state. This drives Q2 and Q3 to the cut-off state, which forces Q4 and subsequently Q6 to saturation and Q5 to cut-off.

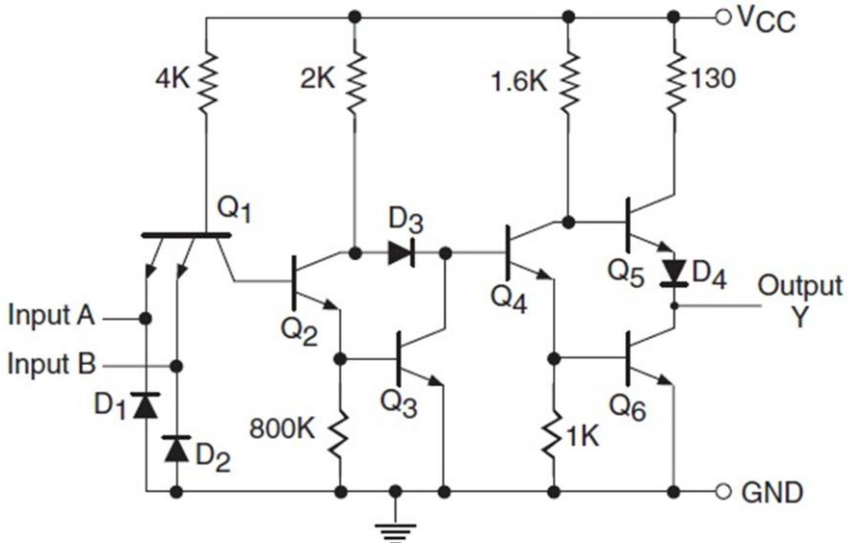


Fig. 19

5- OR Gate

Figure 20 shows the internal schematic of an OR gate in the standard TTL family. The schematic shown is that of one of the four OR gates in a quad two-input OR gate (type 7432/5432). We will begin by investigating the input condition that would lead to a LOW output. A LOW output demands a saturated Q8 and a cut-off Q7. This in turn requires Q6 to be in saturation and Q5, Q4 and Q3 to be in cut-off. This is possible only when both Q1 and Q2 are in saturation. That is, both inputs are in the logic LOW state. This verifies one of the entries of the truth table of the OR gate. Let us now see what happens when either of the two inputs is driven to the HIGH state. This drives either of the two transistors Q3 and Q4 to saturation, which forces Q5 to saturation and Q6 to cut-off. This drives Q7 to conduction and Q8 to cut-off, producing a logic HIGH output.

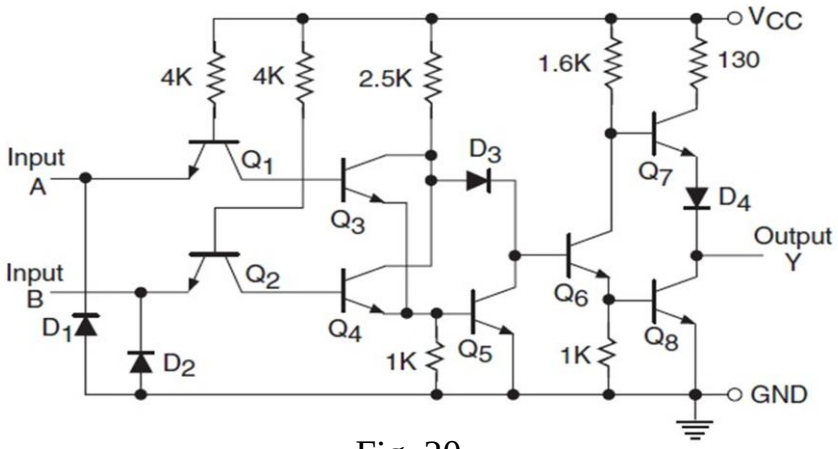


Fig. 20

6- EXCLUSIVE-OR Gate

Figure 21 shows the internal schematic of an EX-OR gate in the standard TTL family. The schematic shown is that of one of the four EX-OR gates in a quad two-input EX-OR gate (type 7486/5486). We will note the similarities between this circuit and that of an OR gate. The only new element is the interconnected pair of transistors Q7 and Q8. We will see that, when both the inputs are either HIGH or LOW, both Q7 and Q8 remain in cut-off. In the case of inputs being in the logic HIGH state, the base and emitter terminals of both these transistors remain near the ground potential. In the case of inputs being in the LOW state, the base and emitter terminals of both these transistors remain near VCC. The result is conducting Q9 and Q11 and non - conducting Q10, which leads to a LOW output. When either of the inputs is HIGH, either Q7 or Q8 conducts. Transistor Q7 conducts when input B is HIGH, and transistor Q8 conducts when input A is HIGH. Conducting Q7 or Q8 turns off Q9 and Q11 and turns on Q10, producing a HIGH output. This explains how this circuit behaves as an EX-OR gate.

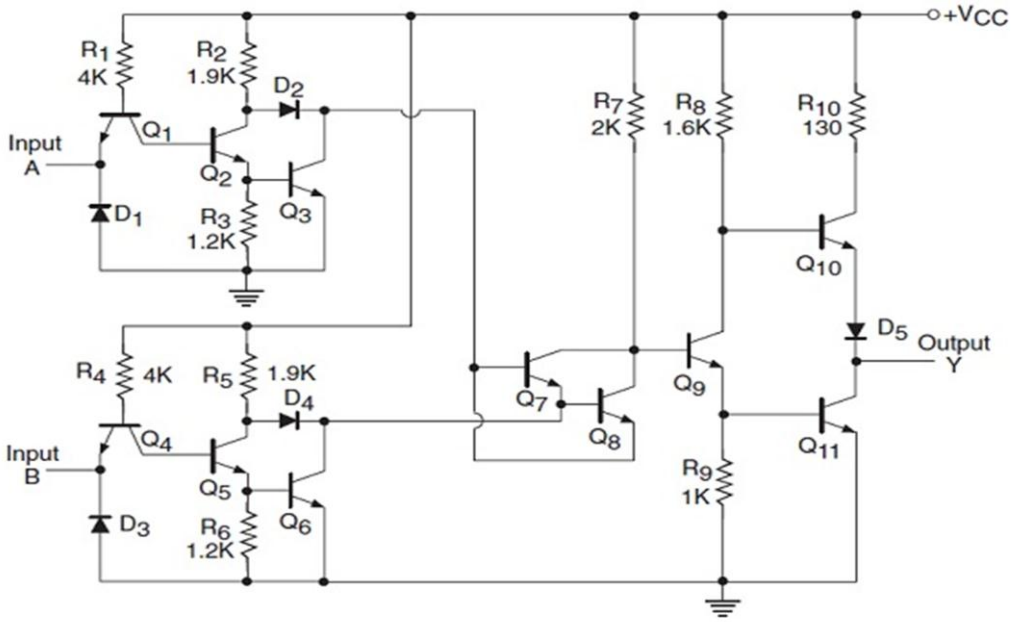

+Vcc
R1
4K
R2
1.9K
D2
Q1
Input
A
Q2
Q3
D1
R3
1.2K
R4
4K
R5
1.9K
D4
Q4
Input
B
Q5
Q6
D3
R6
1.2K
R7
2K
R8
1.6K
R10
130
Q10
D5
Output
Y
Q7
Q8
Q9
Q11
R9
1K

Fig. 21