❖ Data Conversion Circuits

Digital-to-analogue (D/A) and analogue-to-digital (A/D) converters constitute an essential link when digital devices interface with analogue devices, and vice versa. They are important building blocks of any digital system. Before studying types of data conversion the following steps of signal processing must be considered:

❖ Sampling Process

Any signal processing system consists sampling and hold circuits. Sampling operation is a process of taking sufficient number discrete values at a certain points on the waveform, as the number of samples increase, accuracy increase too. To understand the sampling theorem, consider Figure ***1***, which consists of analog signal and sampling pulse waveform. The sampling theorem states "in order to represent an analog signal, the sampling frequency ($f_{samples}$) must be at least twice the highest frequency component (f_{Max}) of the analog signal. Or mathematically:

$$f_{samples} \geq 2f_{Max}$$

All analog signals (except a pure sine wave) contain a spectrum of component frequencies. For a pure sine wave, these frequencies appear in multiplies called harmonics. These harmonics are sine waves of different frequencies and amplitudes, which can be removed using low-pass filter (anti-aliasing filter) since theses frequencies exceed the Nyquist frequency (one-half of the sampling frequency). An alias occurs in this case as illustrated in Figure ***2***; an overlapping appears into the spectrum of the sample waveform. Figure ***3*** shows the effect of low-pass filter in removing the overlap between the frequency spectra of the analog and the sampling signals. Finally, the holding operation must be applied to the filtered signal to make the sampled level be held constant until the next sample occurs. This is necessary for the ***ADC*** have time to process the sampled value. The sampled and hold operation results in a "stair step "waveform. The waveform of the hold operation given in Figure 4.

The two types of signal conversion are:

1- Analog-to-Digital conversion (*ADC*)

An ***A/D*** converter is a very important building block and has numerous applications. It forms an essential interface when it comes to analyzing analogue data with a digital computer. The ***A/D*** conversion process is generally more complex than the D/A conversion process. There are various techniques developed for the purpose of ***A/D*** conversion, and these techniques have different advantages and disadvantages with respect to one another, which have been utilized in the

fabrication of different categories of ***A/D*** converter ***ICs.*** The major performance specifications of an ***A/D*** converter include:

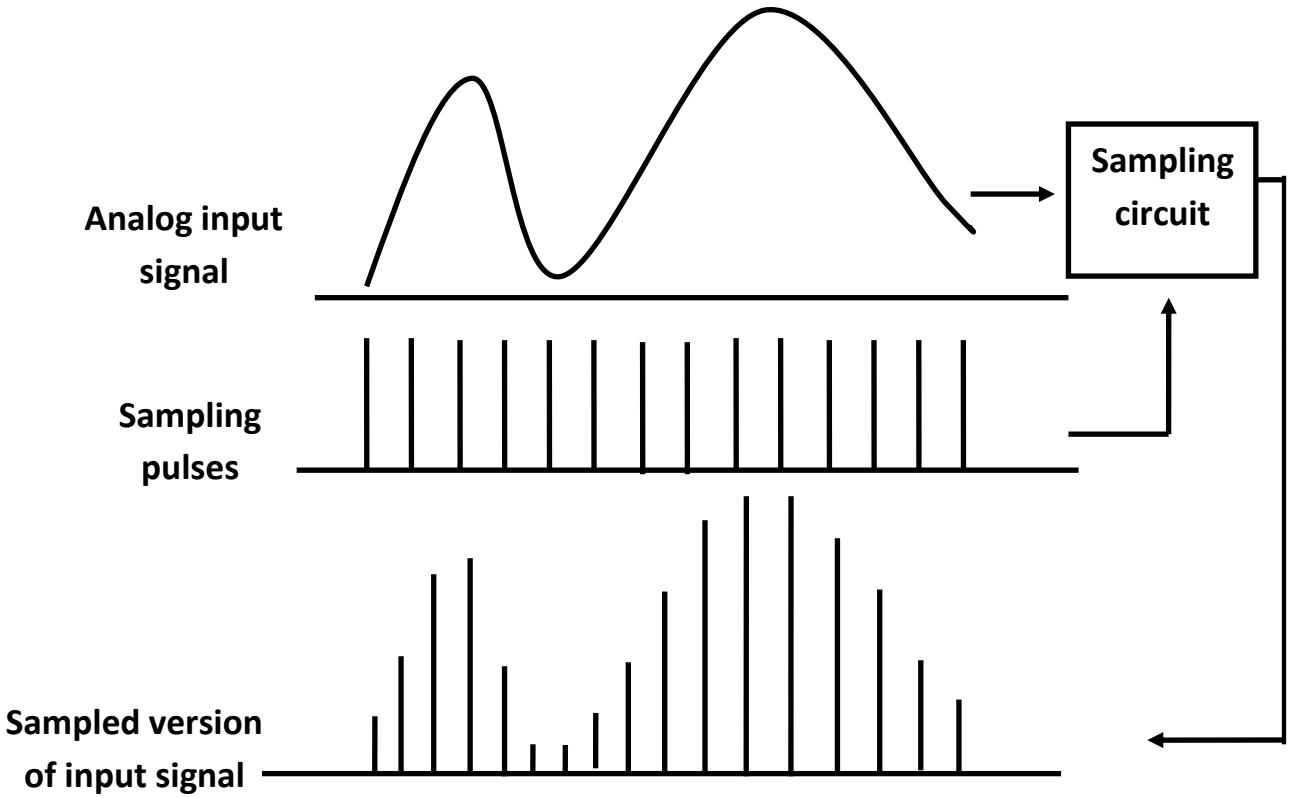


Fig 1 Sampling process

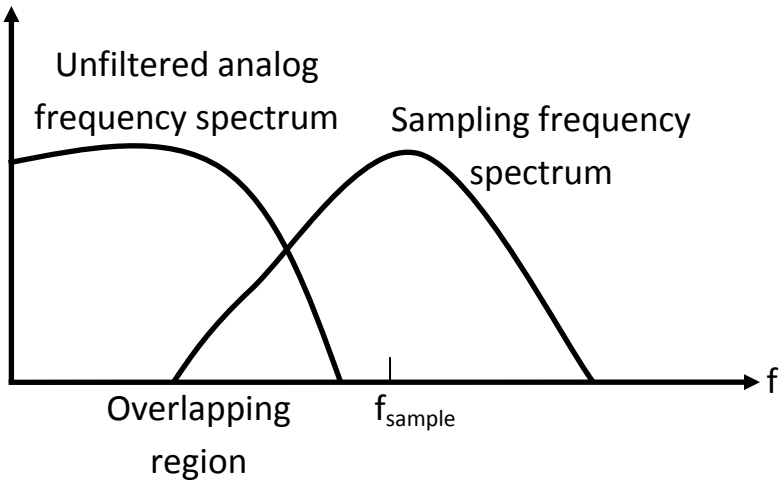


Fig 2 Aliasing effect

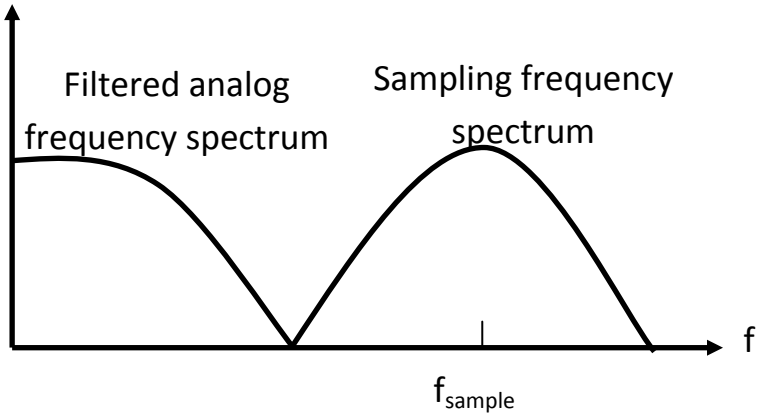


Fig 3 Frequency spectrum after filtering operation

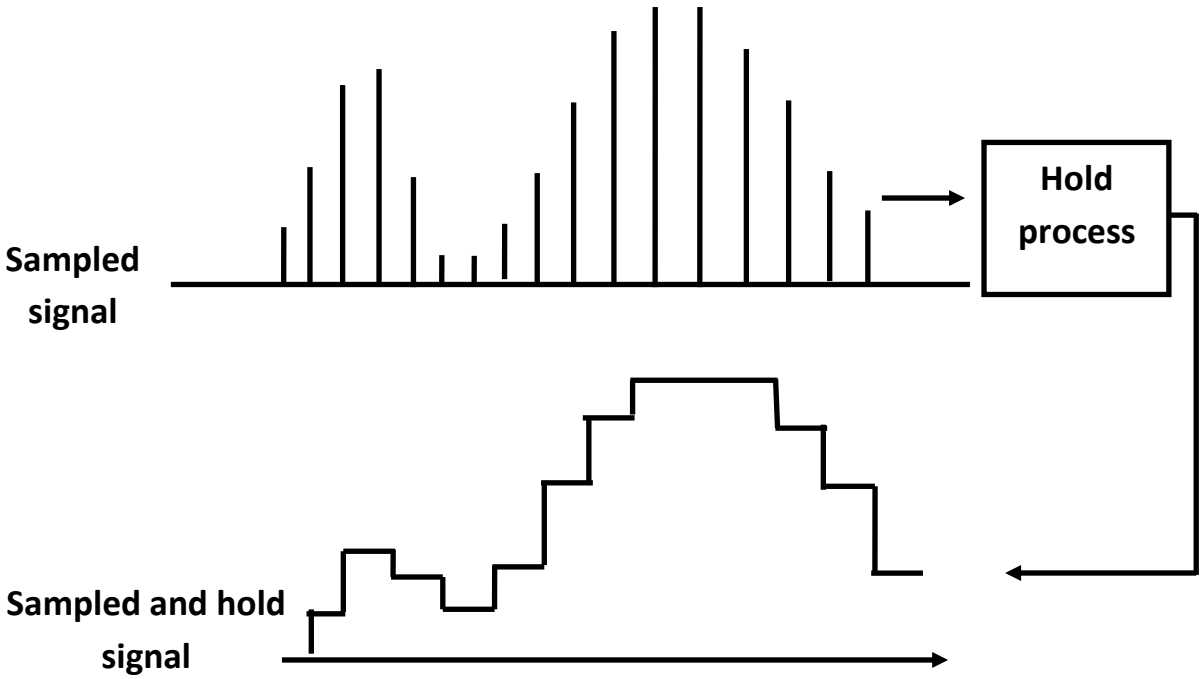


Fig 4 Hold process

✓ **Resolution**

The resolution of an ***A/D*** converter is the quantum of the input analogue voltage change required to increment its digital output from one code to the next higher code. An n-bit ***A/D*** converter can resolve one part in $2^n - 1$. It may be expressed as a percentage of full scale or in bits. The resolution of an eight-bit ***A/D*** converter, for example, can be expressed as one part in ***255*** or as ***0.4%*** of full scale or simply as eight-bit resolution. If such a converter has a full-scale analogue input range of 10 V, it can resolve a 40 mV change in input. In general, for an n-bit D/A converter, the percentage resolution is given by $(1/2n - 1) \times 100$. The resolution in

millivolts for the two cases for a full-scale output of 5 V is approximately 20 mV (for an eight-bit converter) and 1.2 mV (for a 12-bit converter).

✓ **Accuracy**

The accuracy specification describes the maximum sum of all errors, both from analogue sources (mainly the comparator and the ladder resistors) and from the digital sources (quantization error) of the ***A/D*** converter. These errors mainly include the gain error, the offset error and the quantization error.

✓ **Gain and Offset Errors**

The gain error is the difference between the actual full-scale transition voltage and the ideal full-scale transition voltage. It is expressed either as a percentage of the full-scale range (***%*** of ***FSR***) or in LSBs. The offset error is the error at analogue zero for an ***A/D*** converter operating in bipolar mode. It is measured in ***%*** of ***FSR*** or in ***LSBs***.

✓ **Sampling frequency and aliasing phenomenon**

If the rate at which the analogue signal to be digitized is sampled is at least twice the highest frequency in the analogue signal, then the analogue signal can be faithfully reproduced from its quantized values by using a suitable interpolation algorithm. The frequency of an aliased signal is the difference between the signal frequency and the sampling frequency. For example, if sampled at a ***1.5 kHz*** rate, a ***2 kHz*** sine wave would be reconstructed as a ***500 Hz*** sine wave. This problem is called aliasing .

✓ **Quantization error**

The quantization error is inherent to the digitizing process. For a given analogue input voltage range it can be reduced by increasing the number of digitized levels. An ***A/D*** converter having an n-bit output can only identify 2^n output codes while there are an infinite number of analogue input values adjacent to the LSB of the ***A/D*** converter that are assigned the same output code. For instance, if we are digitizing an analogue signal with a peak value of ***7V*** using three bits, then all analogue voltages equal to or greater than ***5.5 V*** and less than or equal to ***6.5V*** will be represented by the same output code, i.e. ***110*** (if the output coding is in straight binary form). The error is ± 0.5 or $\pm$ ***1/2 LSB***, as a one-LSB change in the output corresponds to an analogue change of ***1V*** in this case. The $\pm$***1/2 LSB*** limit to resolution is known as the fundamental quantization error. Expressed as a percentage, the quantization error in an eight-bit converter is one part in ***255*** or ***0.4 %.***

✓ **Nonlinearity**

The nonlinearity specification of an ***A/D*** converter describes its departure from a linear transfer curve. It is expressed as a percentage of full scale or in ***LSBs***.

✓ **Differential nonlinearity**

This indicates the worst-case difference between the actual analogue voltage change and the ideal ***one-LSB*** voltage change. Figure 5 shows the transfer curve for a three-bit ***A/D*** converter with a ***7V*** full-scale range.

✓ **Conversion time**

This is the time that elapses from the time instant of the start of the conversion signal until the conversion complete signal occurs. It ranges from a few nanoseconds for flash-type ***A/D*** converters to a few microseconds for successive approximation type ***A/D*** converters and may be as large as tens of milliseconds for dual-slope integrating ***A/D*** converters.

✓ **Aperture and Acquisition Times**

When a rapidly changing signal is digitized, the input signal amplitude will have changed even before the conversion is complete, with the result that the output of the ***A/D*** converter does not represent the signal amplitude at the start. A sample-and-hold circuit with a buffer amplifier is used at the input of the ***A/D*** converter to overcome this problem. The aperture and acquisition times are the parameters of the sample-and-hold circuit. The signal to be digitized is sampled with an electronic switch that can be rapidly turned ***ON*** and ***OFF***. The sampled amplitude is then stored on the hold capacitor. The ***A/D*** converter digitizes the stored voltage, and, after the conversion is complete, a new sample is taken and held for the next conversion. The acquisition time is the time required for the electronic switch to close and the hold capacitor to charge, while the aperture time is the time needed for the switch completely to open after the occurrence of the hold signal. Ideally, both times should be zero. The maximum sampling frequency is thus determined by the aperture and acquisition times in addition to the conversion time.

✓ **Code width**

The code width is the quantum of input voltage change that occurs between the output code transitions expressed in LSBs of full scale. Code width uncertainty is the dynamic variation or jitter in the code width owing to noise.

❖ ***ADC Methods***

An analog to digital conversion is a process that converts the output of the sampled and holds circuit to the series of logic digits (***zeros*** and ***ones***). The methods of ***ADC*** are:

1. **Simultaneous or Flash A/D Converters**

In this method, input analog signal is compared with a reference voltage. When the analog voltage exceeds the reference voltage,

comparator output is high and the output is low for opposite case. A(***3 bits***) convertor uses seven comparator circuits, ***4 bits*** uses fifteen and so on, generally for ***n*** bits there are (***2^n-1***) comparator circuits. The resistive voltage divider circuit sets the reference voltage for each comparator, this means that the reference voltages (***$V/2^n$, $2V/2^n$, $3V/2^n$, $4V/2^n$…. etc***). Figure 5 shows three bits convertor.

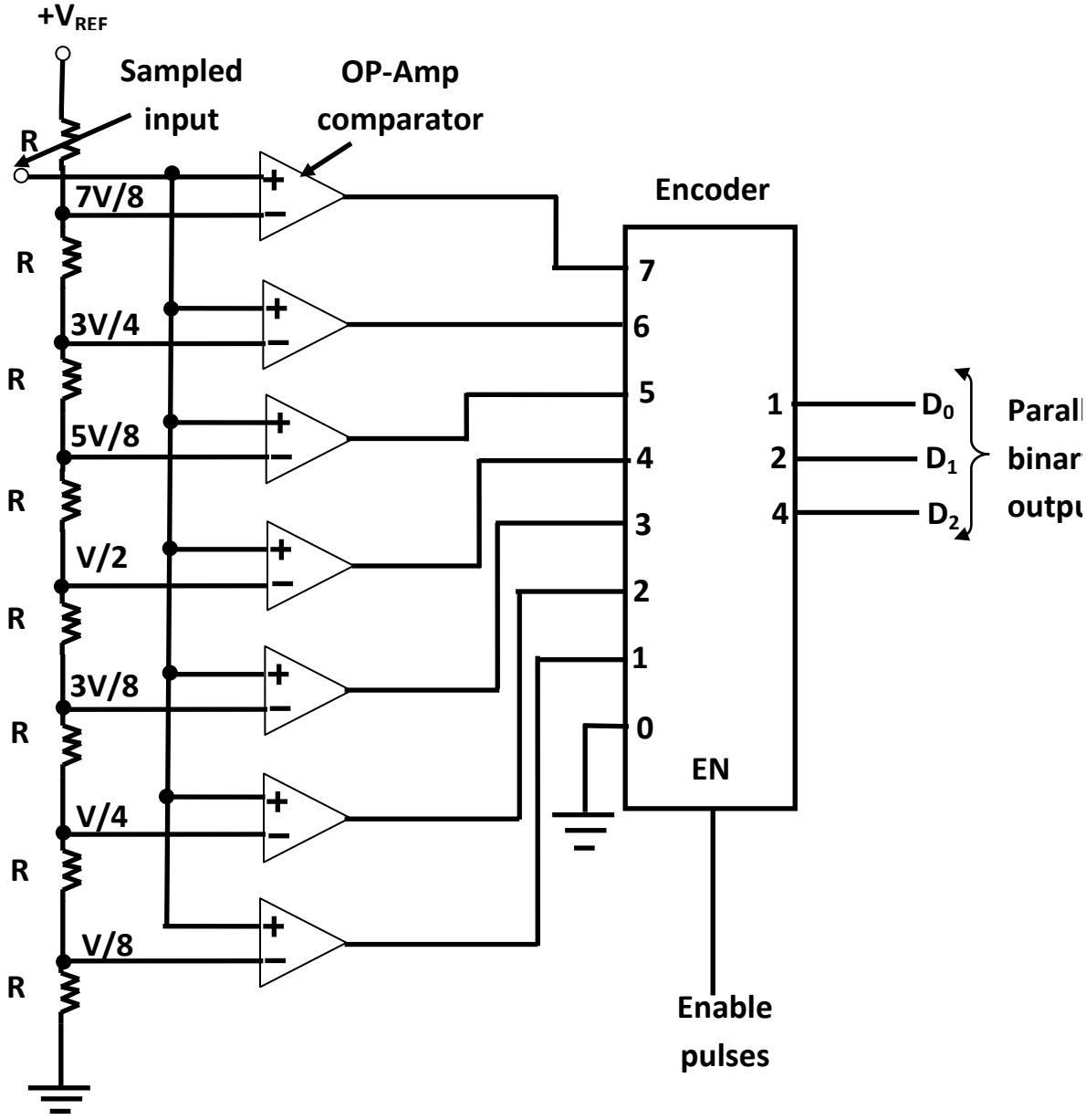


Fig 5 Three bits flash ADC

2. Half-Flash *A/D* Converter

The half-flash ***A/D*** converter, also known as the pipeline ***A/D*** converter, is a variant of the flash-type converter that largely overcomes

the primary disadvantage of the high-resolution full-flash converter, namely the prohibitively large number of comparators required, without significantly degrading its high-speed conversion performance. Compared with a full-flash converter of certain resolution, while the number of comparators and associated resistors is drastically reduced in a half-flash converter, the conversion time increases approximately by a factor of ***two***. For an ***n-bit*** flash converter the number of comparators required is (2^n-1) for encoding of amplitude and one comparator for polarity}, while the same for an equivalent half-flash converter would be $2 \times 2^{n/2}$. In the case of an eight-bit converter, the number is ***32*** (for half-flash) against ***256*** (for full flash).

3. Dual- Slop *ADC*

A dual-slop ADC is common in digital voltmeters and other types of measurement instruments. Figure 6 shows the block diagram of this convertor.

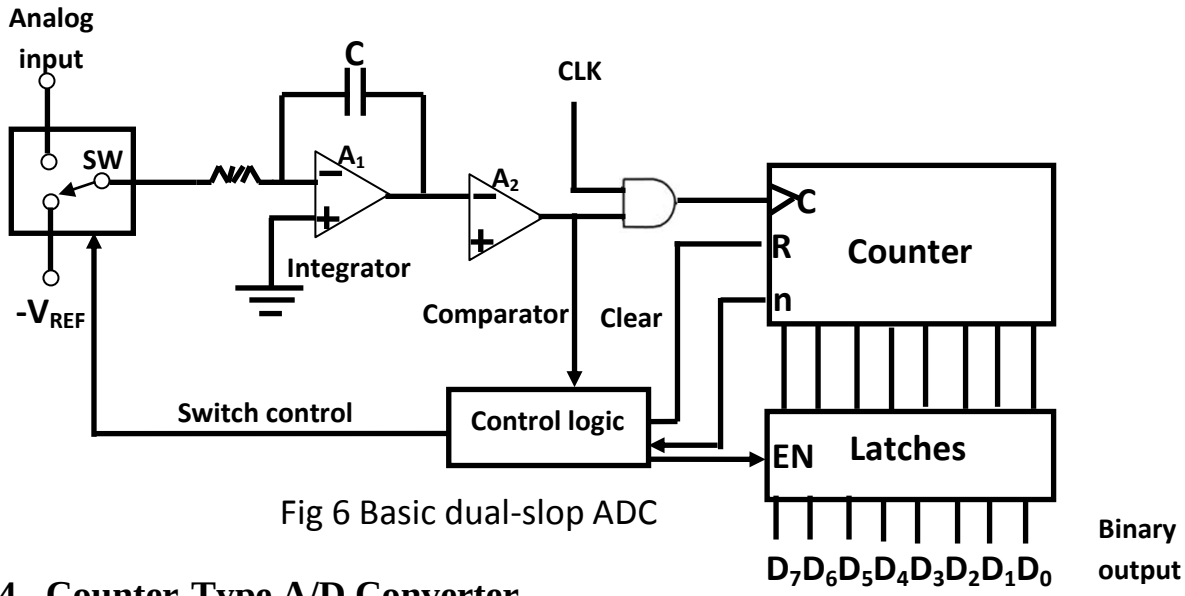


Fig 6 Basic dual-slop ADC

4. Counter-Type A/D Converter

The block diagram of this type is given in Figure 7; the operation of this convertor can be expressed in the following steps:

- The counter is reset (all outputs are zeros)
- The gate is enabled and the clock pulse is applied at the input of the counter
- The output of the counter is applied at the ***DAC*** inputs and the output of DAC is applied to the comparator circuit. When the ***DAC*** output exceeds the input analog signal, the comparator changes state, the gate is disabled and the counter stops. The counter output at that instant of time is then the required digital

output corresponding to the analogue input signal. The advantages of this type are (High resolution and Simplicity). The drawback with this converter is that the required conversion time is longer, it may require as many as 2^n counts before conversion is complete. The average conversion time can be taken to be $2^n/2 = 2^n-1$ counts.

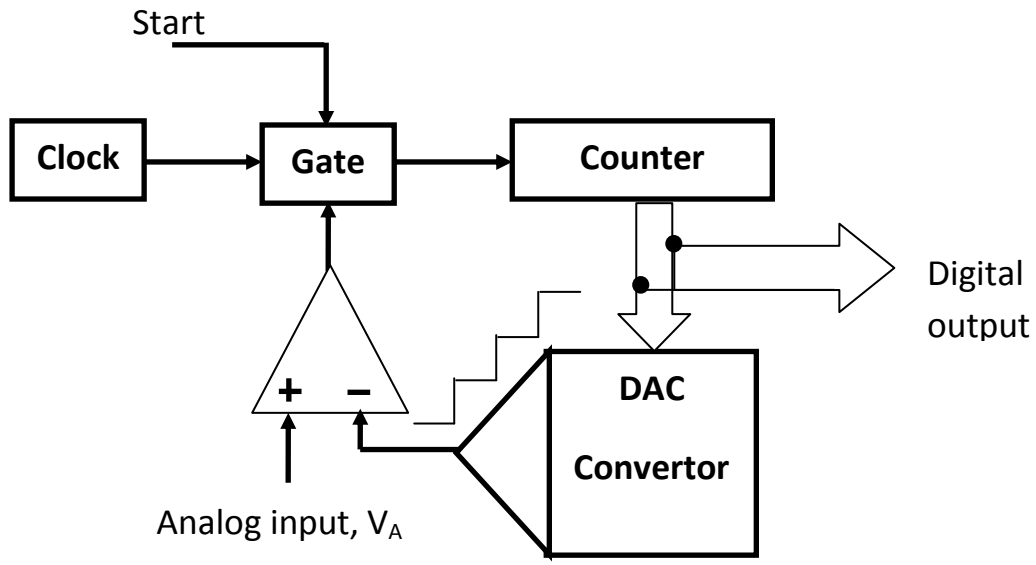


Fig 7 Counter-type A/D

5. Tracking-Type A/D Converter

The tracking-type ***A/D*** converter, also called the delta-encoded ***A/D*** converter, is a modified form of counter-type converter that to some extent overcomes the shortcoming of the latter. In the modified arrangement, the counter, which is primarily an ***UP*** counter, is replaced with an ***UP/DOWN*** counter. It counts in upward sequence whenever the ***D/A*** converter output analogue voltage is less than the analogue input voltage to be digitized, and it counts in the downward sequence whenever the ***D/A*** converter output analogue voltage is greater than the analogue input voltage. In this type of converter, whenever a new conversion is to begin, the counter is not reset to zero; in fact it begins counting either up or down from its last value, depending upon the comparator output. The ***D/A*** converter output staircase waveform contains both positive-going and negative-going staircase signals that track the input analogue signal.

6. Successive Approximation Type A/D Converter

The analogue signal to be digitized by trying only one bit at a time. To illustrate the operation of this type the following example can be considered. For a four-bit successive approximation type ***A/D*** converter, the counter is reset to all ***0s.*** The conversion process is:

- The ***F.F*** that represents the Most Significant Bit (***MSB***) is set.
- The counter output is converted into an equivalent analogue signal and then compared with the analogue signal to be digitized.
- This ***MSB*** either is left in or is to be taken out (the ***F.F*** is reset) according to the compression.
- The clock pulse sets the second ***MSB*** when the first, and repeat second and third steps.
- The process continues until we go down to the ***LSB.***

Figure ***8*** shows a block schematic representation of a successive approximation type ***A/D*** converter.

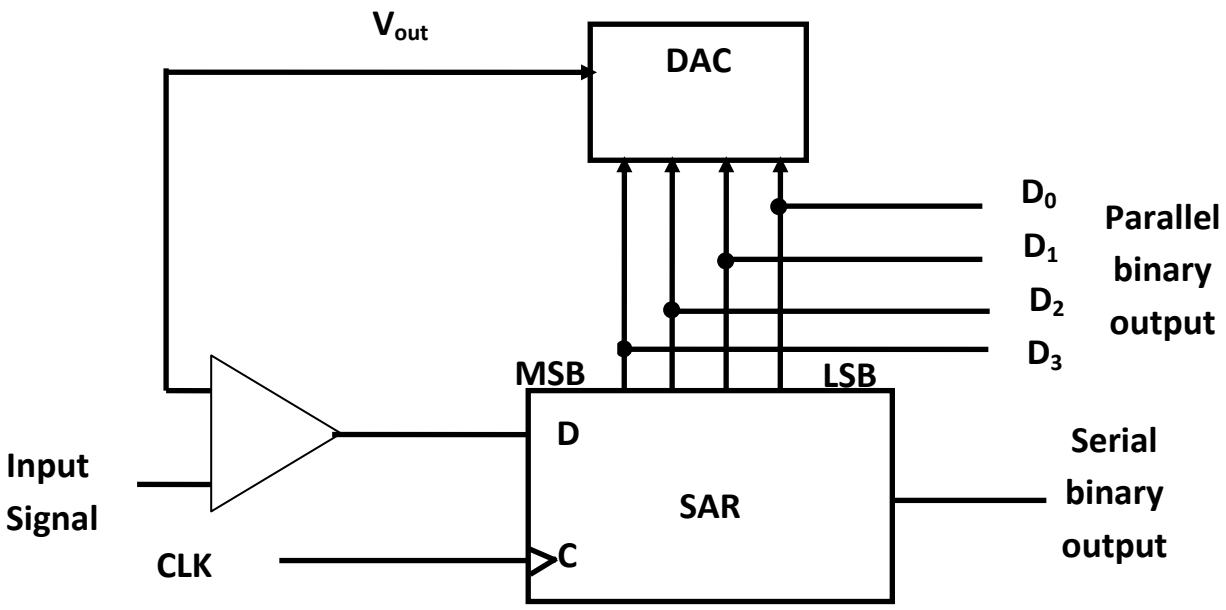


Fig 8 Block diagram of a successive-approximation A/D converter

Figure 9 shows the process of converting (***+3.2V***) in the equivalent digital output.

First step: Since the reference is greater than analog input then the ***MSB*** is set, and this result is greater than (***+3.2V***) then this bit is reset as shown in Figure 9.a.

Second step: The second bit is set and since the reference is less than analog input then the MSB is kept set as shown in Figure 9.b.

Third step: Third bit is set and since the reference is less than analog input then this bit is kept set which represent the digital output.

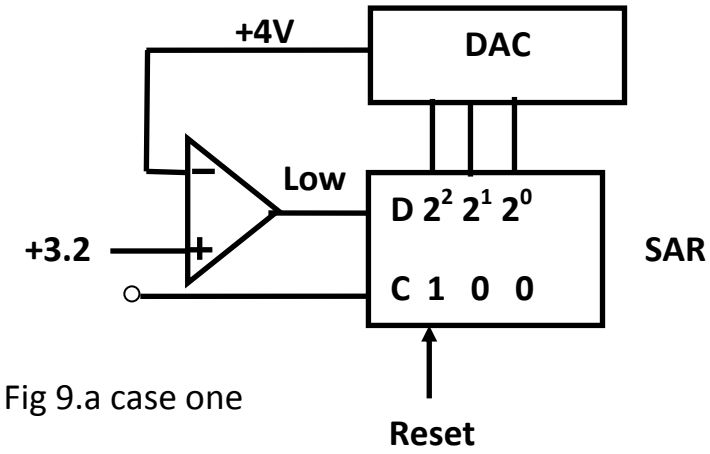


Fig 9.a case one

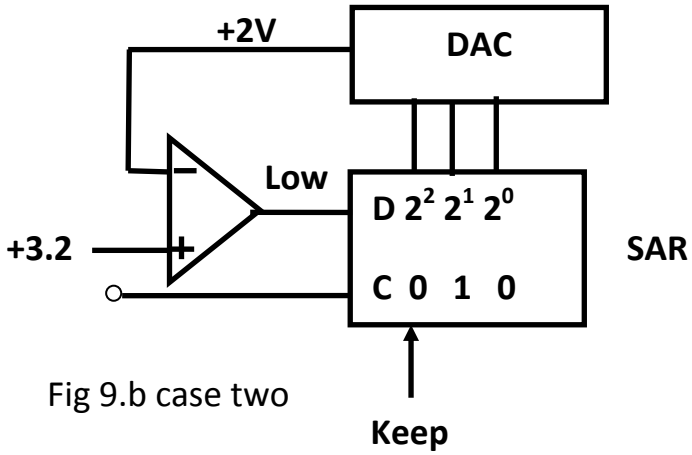


Fig 9.b case two

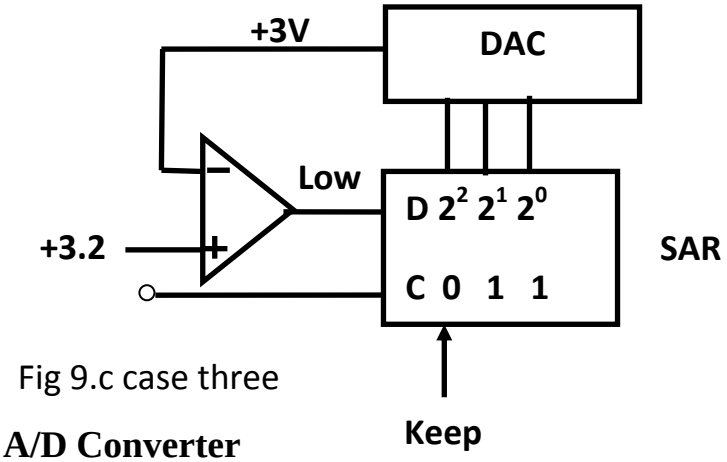


Fig 9.c case three

7. Sigma-Delta A/D Converter

This method is based on delta modulation when the difference between two successive samples (increase or decrease) is quantized. The number of ones over a given number of clock cycles establishes the signal amplitude during that interval. A maximum number of ***ones*** corresponds to the maximum positive input voltage. When the input is zero then there are ones with zeros in the midpoints. For the negative part of input signal, there are no ***ones*** or ***zeros*** in this interval. The block diagram of the

sigma-delta ***ADC*** is given in Figure 10, which consists of ***Σ***, ***DAC***, integrator, ***1-bit*** quantize, ***n-bit*** counter, and latch.

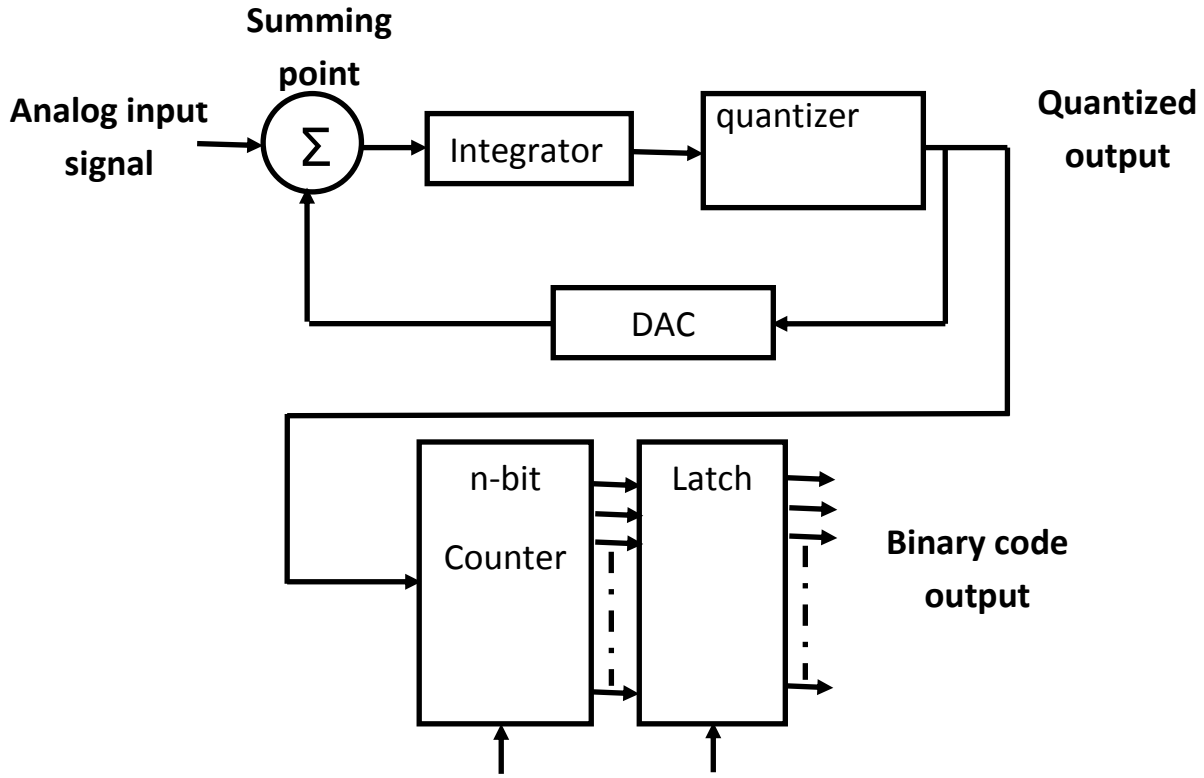


Fig 10 Sigma-Delta A/D Converter

The conversion process is:

- The outputs of ***DAC*** is subtracted from analog input signal
- The difference signal is integrated and the ***1-bit ADC*** increases or decreases the number of ***1s*** depending on the difference signal.
- The bit data stream is converted to a series of binary codes, and these codes are shifted out into the latch for temporary strong.

Ex_1/ for the analog input voltage that illustrated in the following table, find the output digital codes for a flush (***ADC***).

Analog input	1.7	0.8	3.5	4	5.3	2.6	6.6	6.3	4.5	0.1

Sol: Since the maximum value of the input voltage is (***6.6***) then (***3bits***) analog to digital convertor can be used.

The output digits according to the following table

0	V/8	V/4	3V/8	V/2	5V/8	3V/4	7V/8	V
0	1	2	3	4	5	6	7	

This mean that the output codes are:

Analog input	**1.7**	**0.8**	**3.5**	**4**	**5.3**	**2.6**	**6.6**	**6.3**	**4.5**

Output codes	001	000	011	100	101	010	110	110	100

Ex$_2$/ for the output waveform of a flush (***ADC***) that has (V_{REF} = ***10***) is shown in Figure 11, find the range of the input analog voltages.

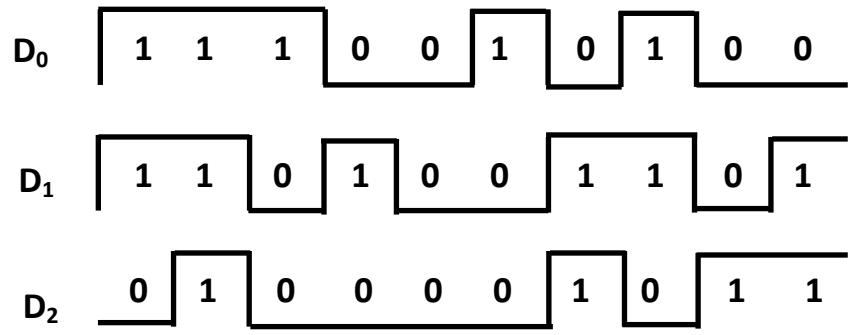


Fig 11 Output waveforms of a flush (ADC)

Sol: the ranges of input analog voltage are:

Digital outputs	Input range
011	15/4 ….. 10/2
111	35/4 ….. 10
001	5/4 ….. 5/2
010	5/2….. 15/4
000	0 ….. 5/4
001	5/4 ….. 5/2
110	15/2 ….. 35/4
110	15/2 ….. 35/4
100	10/2 ….. 25/2
110	15/2 ….. 35/4

HW$_1$: for the waveform of the input analog voltage for a flush (***ADC***) shown in Figure 12 find the output codes.

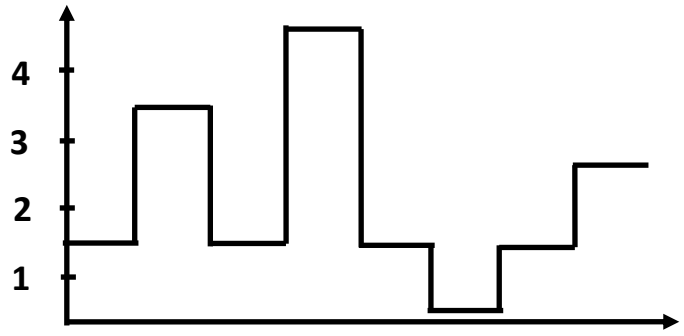


Fig 12 input voltage of a flush ADC

Ex_3/ Determine the conversion time of an ***8-bit A/D*** converter of the counter type shown earlier in Figure 7 for an input clock frequency of ***1 MHz.***

Sol:

An average conversion time equal to half the maximum conversion time is usually defined in the case of such converters.

$TC_{MAX} = 2^n-1$

$= 2^8-1 = 255$ cycles of clock input.

Since the input frequency is (1 MHz) then

The clock time period$=1/(1 \times 10^6)= 1\mu s$.

Therefore, the total maximum conversion time $=255\times1\mu s=255\mu s$

$TC_{AVG}=(255\ \mu s\ /2)=127\ \mu s$.

HW: prove the drawback of the counter ***ADC*** by an example.

0000
0001
0010
0011
0100

Ex_4/ the D/A converter of a counter-type ***A/D*** converter showed in Figure 7 produces a staircase output having a step size of ***10 mV***. The ***A/D*** converter has a ***10-bit*** resolution and is specified to have a quantization error of

Determine the digital output for an analogue input of ***4.012 V***. Assume that the comparator ha$\mp$*1/2 LSB*. on threshold of ***one mV***.

Sol:

Since (***one LSB***) corresponds to ***10 mV*** then (***1/2 LSB***) corresponds to ***5 mV***.

For an analogue input of ***4.012 V***,

Voltage at the other input for the comparator $= 4.012 + V_{threshold}$

$= 4.012+1\times10^{-3}= 4.013V$

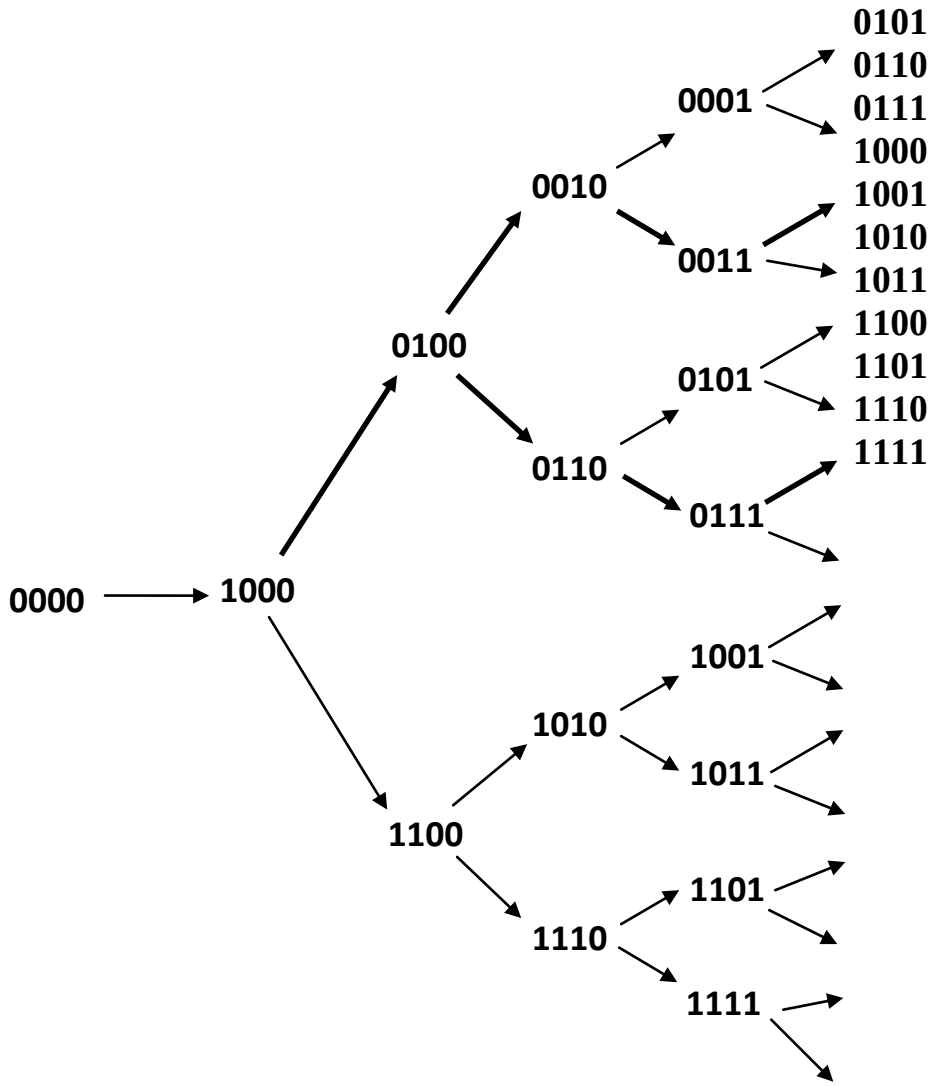
Now, since (***1/2 LSB***) corresponds to ***5 mV*** then the ***D/A*** converter output needs to be ***4.008 V***.

Number of steps $= 4.008/(10\times10^{-3})=400.8 = (401)_{10}$.

Digital output is $(110010001)_2$.

Ex_5/ convert (***6.7 & 2.2***) using successive approximation Type ***A/D*** converter.

Sol: to find the equivalent digital output for (***6.7 & 2.2***) the following diagram can be used.



On the other hand, this example can be solved in the same way that described in the explanation of this ***ADC*** type.

Ex_6/A ***10-bit A/D*** converter of the successive approximation type has a resolution (or quantization error) of ***10 mV***. Determine the digital output for an analogue input of ***4.365 V.***

Sol:

Number of steps= analog input/resolution

$4.365/ (10\times10^{-3}) =436.5$

The A/D converter will settle at step 436.

Digital output is $(0110110100)_2$.

Ex_7/ Compare the average conversion time of an eight-bit counter-type ***A/D*** converter with that of an eight-bit successive approximation type ***A/D*** converter if both are working at a ***10 MHz*** clock frequency.

Sol:

Time period =1/f

= 0.1μs

The average conversion time in the case of a counter-type ***A/D*** converter is given by

TC_{AVG} = [(2^n−1)/2] ×time period

= [(2^8-1)/2] ×0.1μs

=12.75μs.

The conversion time in the case of a successive approximation type ***A/D*** converter is given by

TC_{AVG} = n ×time period

= 8×0.1 μs = 0.8 μs

=12.12 μs

2- Digital -to- Analog conversion (*DAC*)

Once the analog signal has been converted to the digital form, it can be converted to the analog form again according to the application and need. Generally there are some types of ***DAC*** which are:

1. Multiplying-type D/A converters

In a multiplying-type ***D/A*** converter, the converter multiplies an analogue reference by the digital input. Figure 13 shows the block diagram of this type. Some ***D/A*** converters can multiply only positive digital words by a positive reference. This is known as single quadrant (***QUAD-I***) operation. Two-quadrant operation (***QUAD-II*** and ***QUAD-III***) can be achieved in a ***D/A*** converter by configuring the output for bipolar operation.

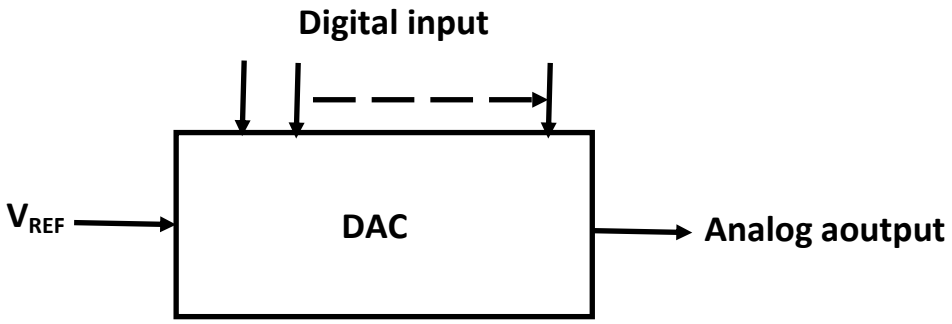


Fig 13 Block diagram of DAC

Multiplying ***D/A*** converters are particularly useful when we are looking for digitally programmable attenuation of an analogue input signal.

2. Bipolar-output *D/A* converters

In bipolar-output ***D/A*** converters the analogue output signal range includes both positive and negative values. The transfer characteristics of an ideal two-quadrant bipolar-output ***D/A*** converter are shown in Figure 14.

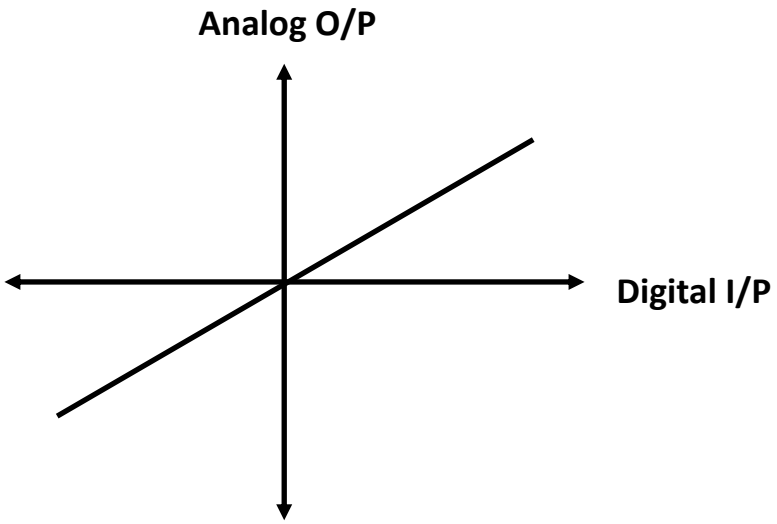


Fig 14 Ideal two-quadrant bipolar-output D/A converter

The following circuits that used to convert the digital signal to the analog form are:

☒ **Binary-Weighted- Input Digital- to- Analog Convertor**

This method uses a resistor network that connected together as illustrated in Figure 15 the resistors are { ***R*** corresponds to the highest binary-weighted input (2^n), ***2R*** corresponds to the (2^{n-1}), …….. ***nR*** corresponds to the 2^0}. The disadvantage of this DAC is the number of different resistor values and the fact that the voltage level must be the same of the input.

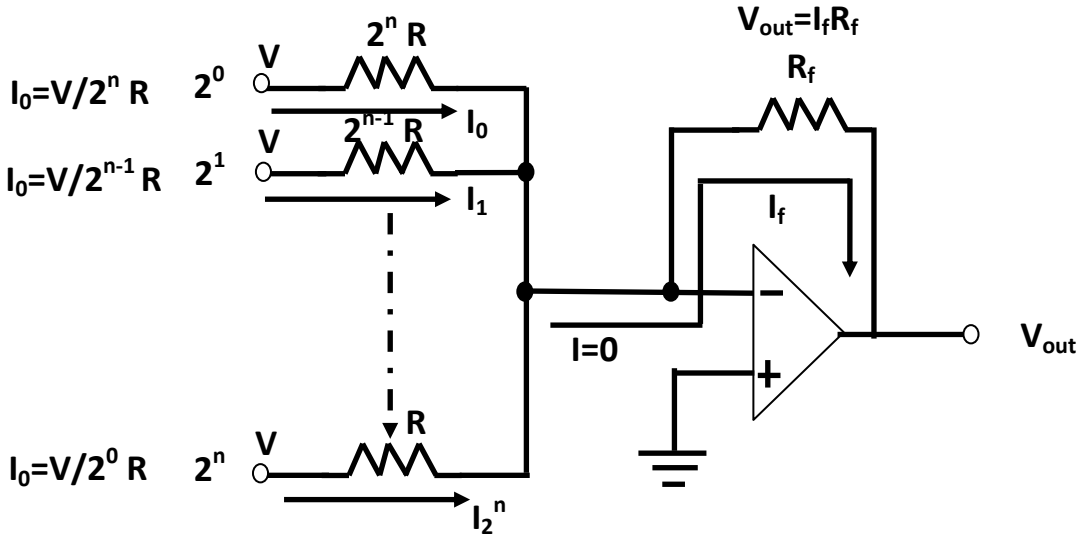


Fig 15 n bits binary- weighted- input DAC

☒ R/2R Ladder Digital- to- Analog Convertor

In this method, two resistor values are used and connected as shown in Figure 16. This configuration solves the problem of binary-weighted-input ***DAC*** method.

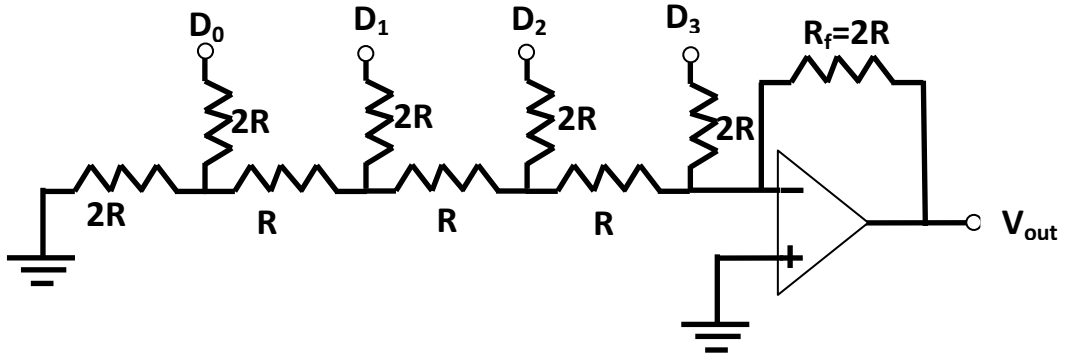


Fig 16 four bits R/2R Ladder

D/A converters are usually operated in either of the following two modes of operation, which are (Current steering mode and Voltage switching mode)

1. Current Steering Mode of Operation

In the current steering mode of operation of a ***D/A*** converter, the analogue output is a current equal to the product of a reference voltage and a fractional binary value ***D*** of the input digital word. The output current is often converted into a corresponding voltage using an external op-amp wired as a current-to-voltage converter. Figure 17 shows the circuit arrangement of the four-bit ***D/A*** converter. The ***R/2R*** ladder network divides the input current I due to a reference voltage V_{ref} applied at the reference voltage input of the ***D/A*** converter into binary weighted currents, as shown. These currents are then steered to either the output designated ***Out-1*** or ***Out-2*** by the current steering switches. The positions of these current steering switches are controlled by the digital input word. Logic '***1***' steers the corresponding current to ***Out-1***, whereas logic '0' steers it to ***Out-2***. In general, the maximum analogue output voltage is given by – $(1-2^{-n}) \times V_{ref}$, where n is the number of bits in the input digital word.

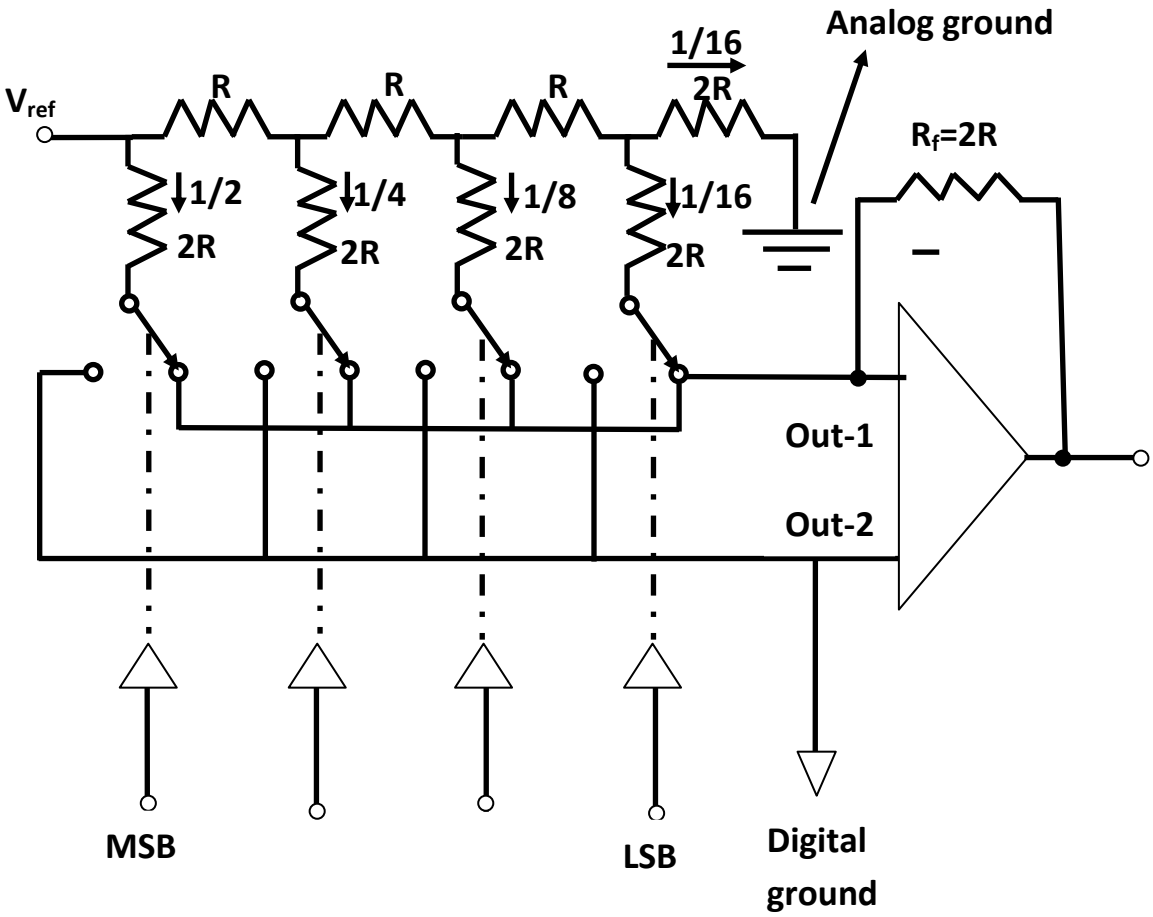


Fig 17Current steering mode four-bit D/A converter

2. Voltage Switching Mode of Operation

In the voltage-switching mode of operation of a (***R/2R***) ladder type ***D/A*** converter, the reference voltage is applied to the ***Out-1*** terminal and the output is taken from the reference voltage terminal. ***Out-2*** joined to analogue ground. Figure 18 shows a four-bit ***D/A*** converter of the ***R/2R*** ladder type in voltage switching mode of operation.

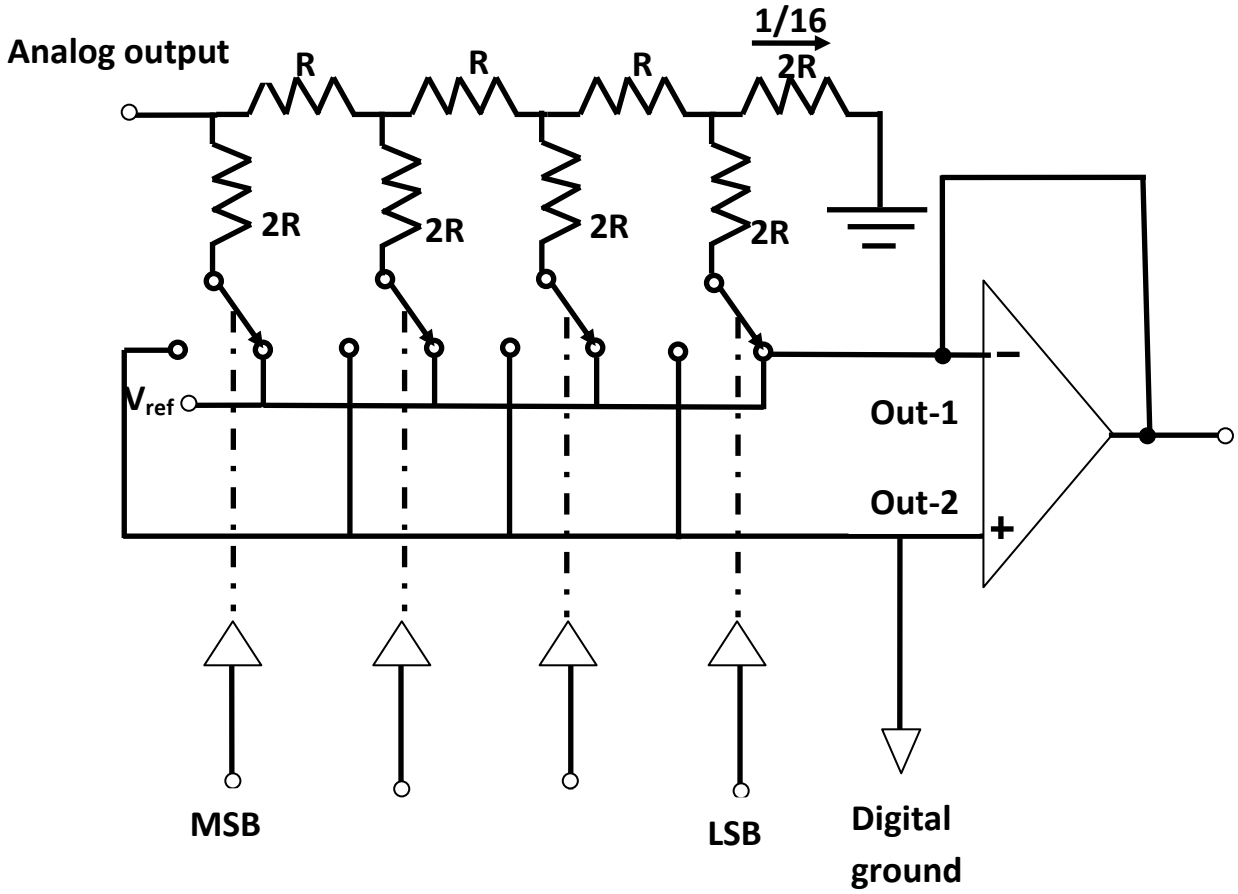


Fig 18 Voltage steering mode four-bit D/A converter

The output voltage is the product of the fractional binary value of the digital input word and the reference voltage applied at the ***Out-1*** terminal, i.e. ($D.V_{ref}$).

The major performance specifications:

1- Resolution

For ***n-bits DAC***, the resolution can be found from the following equation [Resolution= $(1/2^n - 1) \times 100$].

2- Accuracy

The accuracy of a ***D/A*** converter is the difference between the actual analogue output and the ideal expected output when a given digital input is applied. For example, if a converter has a full- scale of ***10V*** and accuracy is ***0.01% the maximum error = 10V* 0.001 =10mV***.

3- Conversion Speed or Settling Time

The conversion speed of a ***D/A*** converter is expressed in terms of its settling time. The settling time is the time period that has elapsed for the analogue output to reach its final value within a specified error band after a digital input code change has been effected.

4- Dynamic Range

This is the ratio of the largest output to the smallest output, excluding zero, expressed in dB. For linear ***D/A*** converters it is (***20×log$_2^n$***), which is approximately equal to ***6n***.

5- Nonlinearity and Differential Nonlinearity

Nonlinearity (***NL***) is the maximum deviation of analogue output voltage from a straight line drawn between the end points, expressed as a percentage of the full-scale range or in terms of ***LSBs.*** Differential nonlinearity (***DNL***) is the worst-case deviation of any adjacent analogue outputs from the ideal ***one-LSB*** step size.

Ex$_8$/ An ***eight-bit D/A*** converter produce an analogue output of ***12.5 mV*** for a digital input of ***00000010***. Determine the analogue output for a digital input of ***00000100***.

Sol:

The currents for the branches in the case of eight current steering model are: $\{\frac{1}{2}, \frac{1}{4}, \frac{1}{8}, \frac{1}{16}, \frac{1}{32}, \frac{1}{64}, \frac{1}{128}, \frac{1}{256}\}$

Since for 00000010, the output is (12.5 mV) then

$V_{output} = V_{ref}/128 \Longrightarrow V_{ref} = 128\times12.5mV$

$= 1.6V$

For 00000100 the output voltage can be found as:

$V_{output} = 1.6/64$

$= 25mV.$

Ex$_9$/ find the resolution in millivolts of eight & twelve bits DAC for a full-scale output of 5V.

Resolution = $1/2^n$ ×full-scale output

For 8-bits

Resolution = $1/2^8 \times 5V$

= 0.0195V or approximately = 20 mV.

For 12-bits

Resolution = $1/2^{12} \times 5V$

= 0.0012207V or approximately = 1.2 mV.

Ex$_{10}$/ An ***eight-bit D/A*** converter has a step size of ***20 mV***. Determine the full-scale output and percentage resolution.

Sol:

Since $(1/2^8) \times V = 20 \times 10^{-3}$ then

$V = 20 \times 10^{-3} \times 2^8 = 5.12V.$

The full-scale output = $[(2^n - 1)/2^n] \times V = [(28 - 1)/28] \times 5.12 = (255/256) \times 5.12 = 5.1V.$

Percentage resolution = $[1/(2^n - 1)] \times 100$

$= 100/255 = 0.392\%.$

Or Percentage resolution = Step size/full-scale output × 100
= $(20 \times 10^{-3}/5.1) \times 100 = 0.392$ %.

Ex_{11}/ A certain ***eight-bit D/A*** converter has a full-scale output of ***5 mA*** and a full-scale error of $\pm$ ***0.25%*** of full scale. Determine the range of expected analogue output for a digital input of ***10000010.***

Sol:

Step size = Full-scale output/Number of steps
$= 5\times10^{-3}/2^{8}-1$
= 19.6 μA

For a digital input of 10000010 = 130_{10} the analogue output is given by $130 \times 19.6 = 2.548$ mA.

Error = $\mp$ $0.25\times5\times10^{-3}/100$
= $\mp$ 12.5 μA

The range of the expected analogue output is (2.5355–2.5605 mA).

HW_2/ A ***12-bit D/A*** converter has a resolution of ***2.44 mV***. Determine its analogue output for a digital input of ***111111111111.***

Ex_{12}/ find the analog output of ***4-bit*** binary- weighted- input ***DAC*** if the waveform of digital input is given in Figure 19. Note that ***R = 25kΩ & R_f =10 kΩ.***

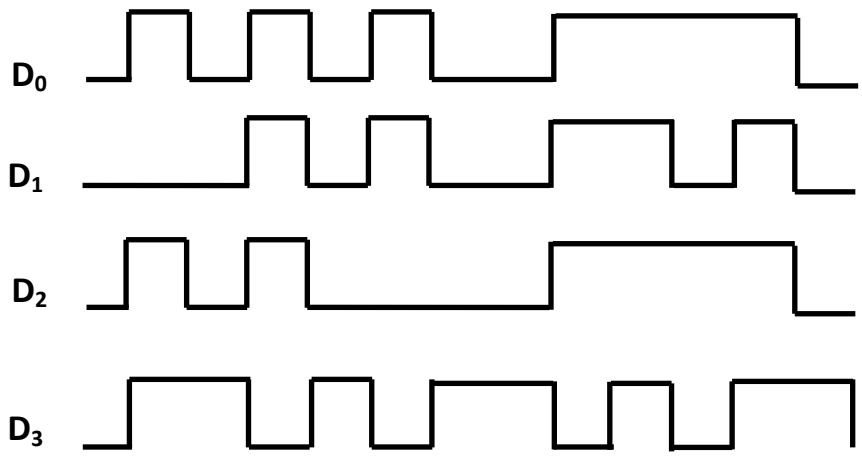


Fig 19 Waveform of a four DAC

Sol: the circuit of such ***DAC*** is given in Figure 20

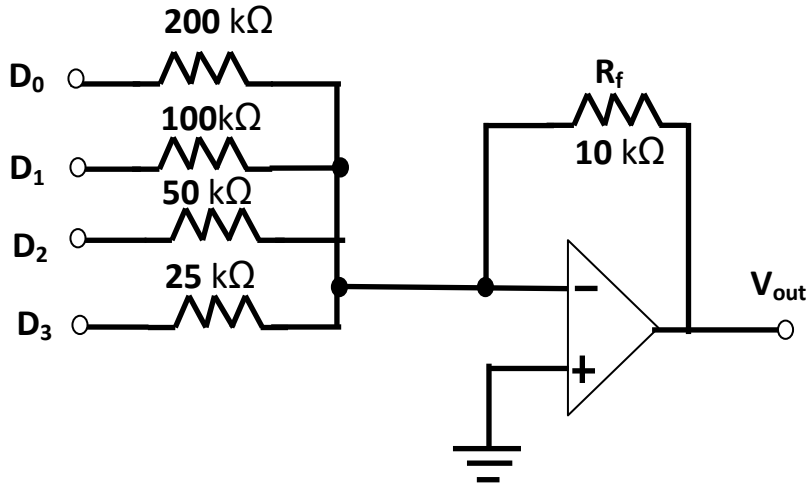


Fig 20 Four bits binary- weighted- input

The currents of branches are:

$I_0 = \frac{5V}{200K\Omega} = 0.025A$

$I_1 = \frac{5V}{100K\Omega} = 0.05mA$

$I_2 = \frac{5V}{50K\Omega} = 0.1mA$

$I_3 = \frac{5V}{25K\Omega} = 0.2mA$

The output voltages result from these currents are:

$V_{out}(D_0) = 10k\Omega \times (-0.025mA) = -0.25V$, $V_{out}(D_1) = -0.5V$, $V_{out}(D_2) = -1V$, and $V_{out}(D_3) = -2V$

From wave forms of digital inputs, input sequences are:

0000	0001	1110	0001
1011	1100	1111	
0001	0001	1010	
1110	0001	1111	

According to the waveforms the output voltage is given in Figure 20:

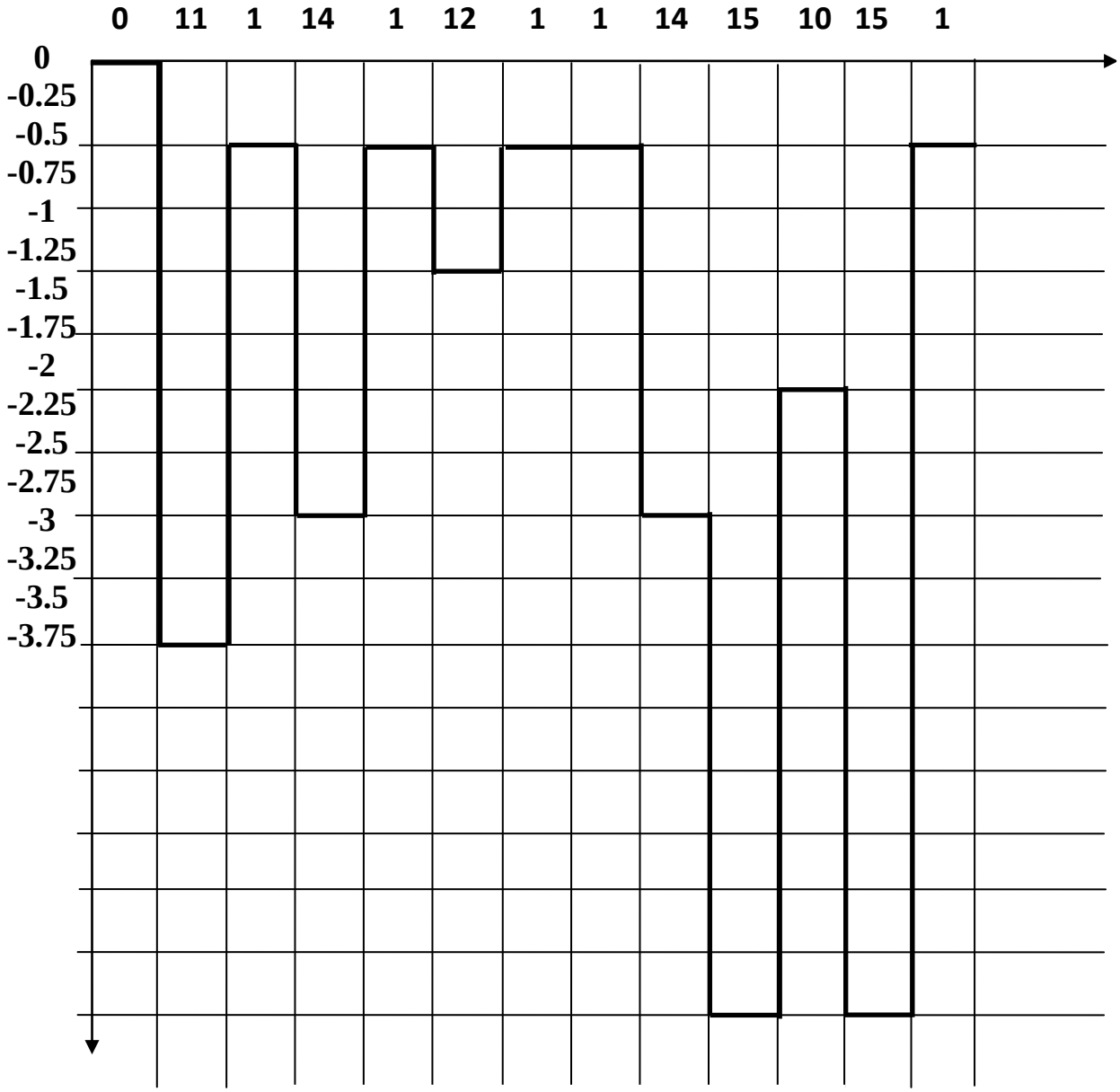


Fig 20 Output voltage waveform

Ex13/ find the output voltages for the ***3-bits R/2R*** ladder ***DAC*** has digital input as shown in Figure 21.

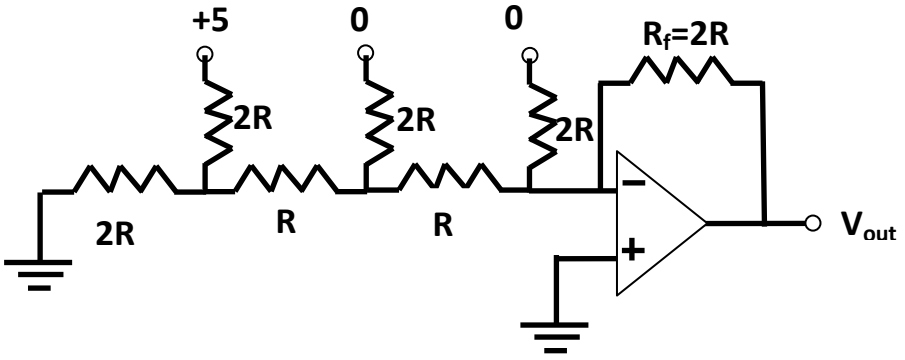


Fig 21 Three bits R/2R Ladder DAC with 001 input digits

Sol: when D_0 =+5, D_1=0, and D_2=0 then the equivalent circuit will be as shown in Figure 22.

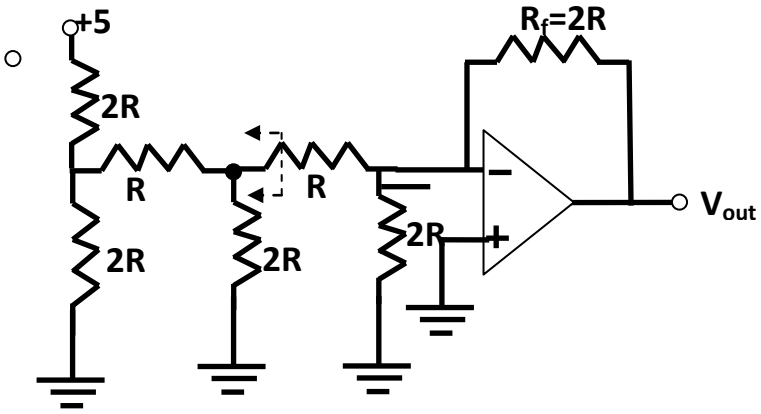
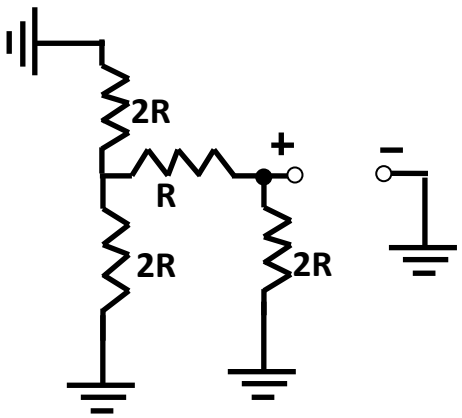
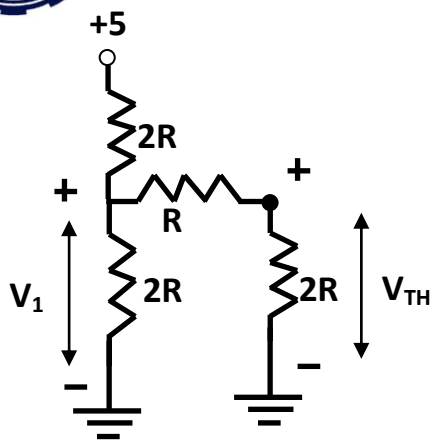


Fig 21 Three bits R/2R Ladder DAC with 001 input digits

To solve above circuit, apply Thevenin's theorem across the bold poin showed in Figure 21

R_{TH} = ([(2R ‖ 2R) + R] ‖ 2R)
R_{TH} = R
In addition, V_{TH} can be found as follow





R_{eq} = [((R+2R) ‖2R) +2R]
$= \frac{16}{5}$ R Ω
$I_T = \frac{5*5}{16R}$
$= \frac{25}{16R}$ A
$V_1 = \frac{6}{5}R* \frac{25}{16R}$
= 1.875V
I= (1.875/3R)
=(0.625/R) A
V_{TH} = 2R*(0.625/R)
= 1.25V
The equivalent circuit is illustrated in Figure 22

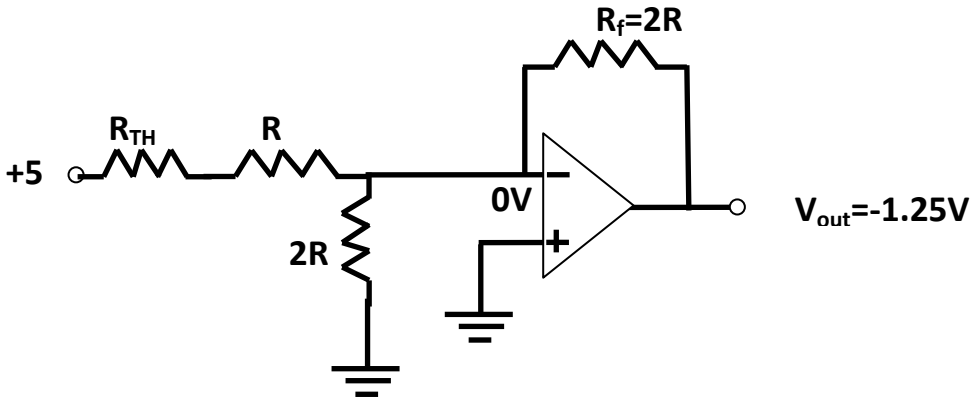


Fig 21 Equivalent circuit for 001 digital input

HW_3: for the following digital inputs {***1000. 0010, 1001, 0000, 0001, 1111, 1110, 1100, 1101***}, draw the output voltage for binary- weighted-input ***DAC*** if ***R = 10KΩ, R_f =5 KΩ***.
HW_4: design a three-bits binary- weighted- input ***DAC*** for input digits (***011)2, I2=0.25mA, and V_{out} =-3V***.
HW_5: for the waveform shown in Figure 22 of input digits for ***3-bits R/2R Ladder DAC***, draw the output waveform.

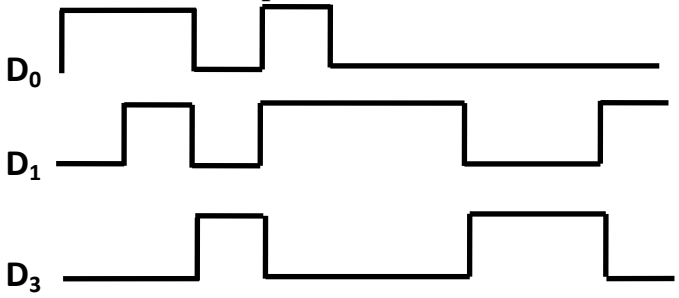


Fig 22 Waveforms of input digits for three bits R/2R Ladder DAC

HW$_6$: design a ***4-bits R/2R Ladder DAC*** for input digits $(010)_2$, V_{out} ***=-6V,*** and I_{TH} ***= 1.5mA.***

❖ DAC errors:

Some errors occur when the digital signals convert into the analog form. These errors are:

- No monotonicity

In particular case, the error occurs because the 2^1***bit*** in the binary code is interpreted as a constant ***0***. To illustrate this error, consider the following example.

Ex14/ for the circuit of ***3-bits*** binary- weighted- input ***DAC*** shown in Figure 23, illustrate the nonmonotonicity error for the sequence {***0,1,2,3,4,5,6,7***}.

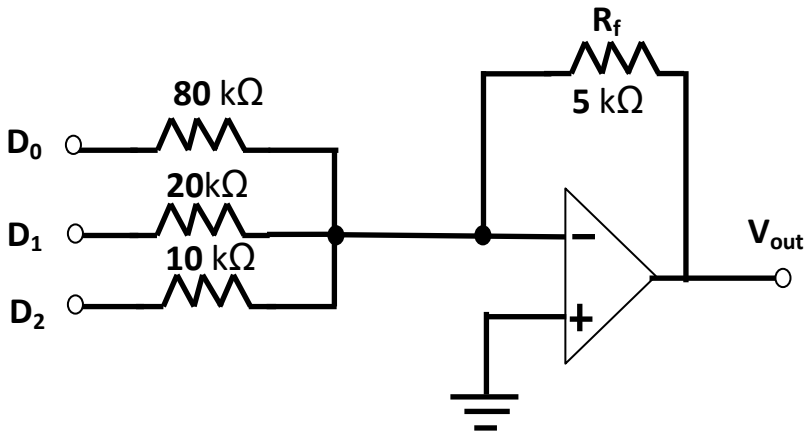


Fig 23 three bits binary- weighted- input

When D_0 = 5V then I_0 = 0.0625mA, D_1 =5 V then I_1= 0.25mA, and when D2 =5V then I_2 = 0.5mA.The output voltages can be calculated as:
$V_{out}(D_0)$ = -0.3125V
$V_{out}(D_1)$ = -1.25V
$V_{out}(D_2)$ = -2.5V.The output voltages in ideal and practical case are illustrated in the following table:

Input sequence	Ideal output voltage	Practical output voltage
000	**0V**	**0V**
001	**-0.3125V**	**-0.3125V**
010	**-1.25V**	**0V**
011	**-1.5625V**	**-0.3125V**
100	**-2.5V**	**-2.5V**
101	**-2.8125V**	**-2.8125V**
110	**-3.75V**	**-2.5V**
111	**-4.0625V**	**-2.8125V**

- Differential Nonlinearity

This error occurs when the step amplitude is less than should be for a certain input codes. This particular output could be caused by ***2^2bit*** having an insufficient weight. In addition, the steps can be greater than normal if a particular binary weight were greater than it should be.

- Low or High Gain

In this case, low gain appear when all of the step amplitudes are less than ideal, while in the case of high gain, all of the step amplitudes are greater than ideal. A faulty feedback resistor in the ***Op-amp*** circuit causes this error.

- Offset Error

This error occurs when the output of zero digital input, the output voltage is nonzero. This offset error is the same for all steps in the conversion.