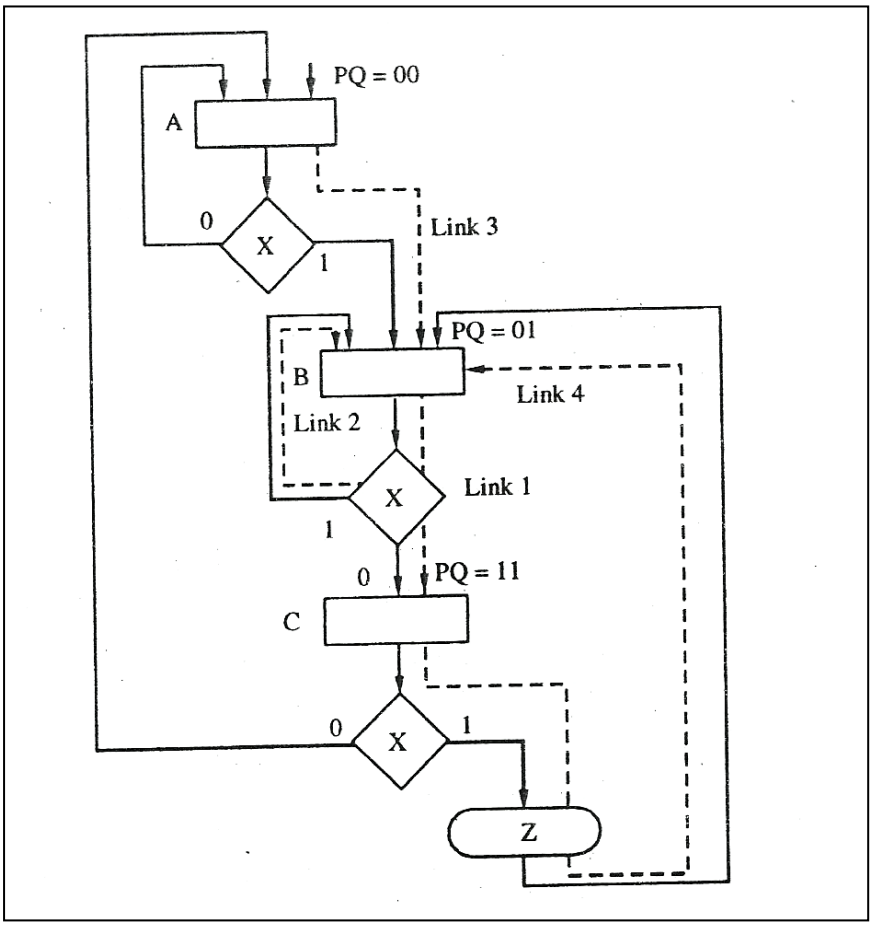
Realization Of ASM Charts

Realization of ASM charts are similar to the realize state diagram .The following procedure can be used to derive the next state equation for a flip-flop Q .if gates and flip-flops are used .

1. The first step is to make a suitable state assignment for each state
2. Search all the states for which Q is one .
3. For each of these states, find all of the link paths that lead into the state.
4. For each of these link paths ,find a term that is 1 when the link path .
5. The expression for the next state of Q is formed by ORing together all the terms found in step3.
6. Similarly ,the expression for output can be read directly from the ASM chart.
7. Find a simplified expression for output and next-state equations with a K-map using the unused state assignment as a don't care condition.
8. Realize the SM chart using gates and flip-flops.

Example

For the SM chart of Fig. below make the following state assignment for the flip flops P and Q.



Solution

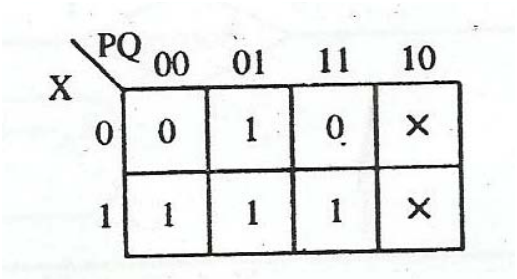
Z=PQX

$Q^+ = P'QX' + P'QX + P'Q'X + PQX$

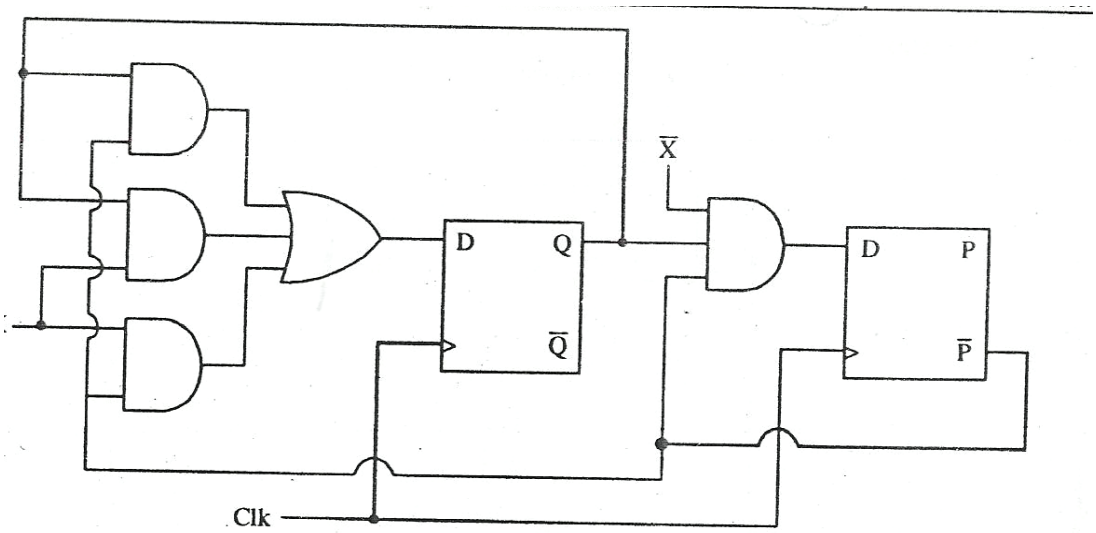
link1 link2 link3 link4

$P^+ = P'QX'$ link1

Next state equation of Q can be simplified with k-map using the unused state assignment as a don't care condition .



$Q^+ = P'Q' + P'X + QX$



Controller Design

System controller is a special sequential circuit that receives input from each components of the system and outer interface and generate the control signals that control whole system The methods of design as the following:

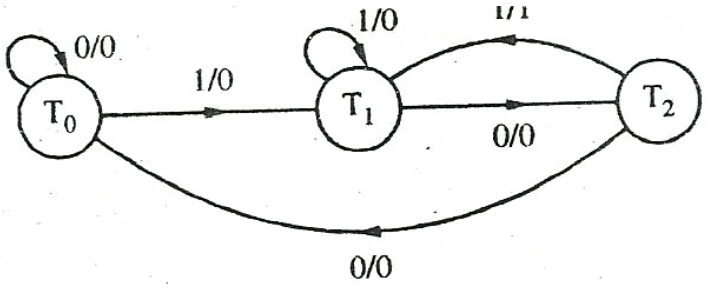
1. **Using JK flip-flops** .The following procedure can be used for controller designing using JK flip-flops.
    - The first step is to assign binary values to each state in the ASM chart .
    - Obtain the state table for a controller .A state table for a controller is a list of present states,inputs ,their corresponding next states and outputs .The inputs are taken

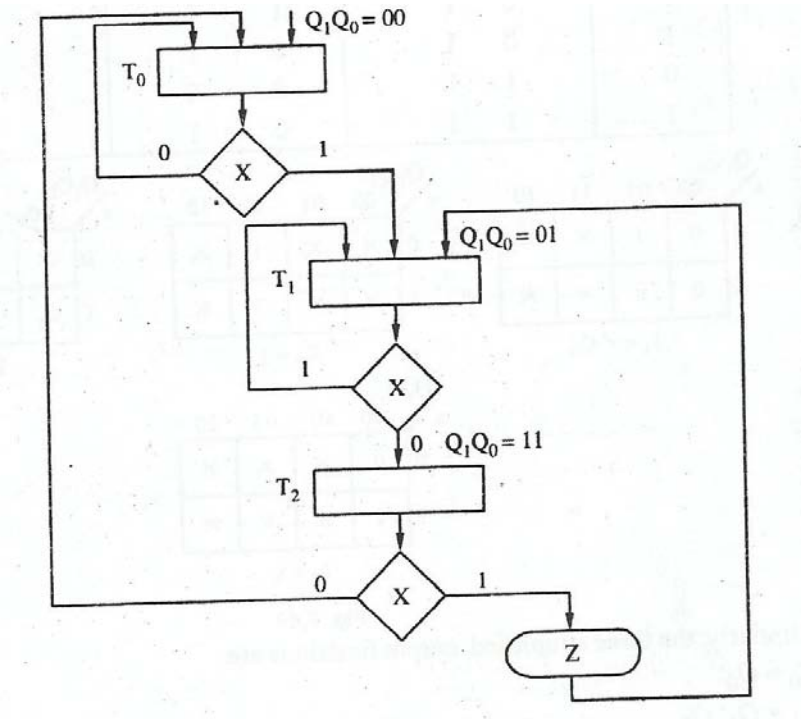
from the conditions in the decision boxes of the ASM chart .The outputs are equivalent to the present state of the control.

- Obtain the excitation table of the flip-flop inputs.
- Find a simplified expression for output and the following example.
- Realize the control unit using gates and flip-flops.

Example

Draw an ASM chart and state diagram to describe a sequence detector that detects a sequence of 101 .Design the control unt using JK flip-flop





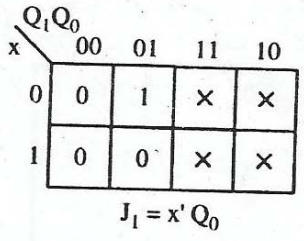
The state corresponding to the ASM chart (Fig.above)is show in Table

Present State Symbol	Present State	Input	Next State	Output
	$Q_1\ Q_0$	x	$Q_1\ Q_0$	$T_0\ T_1\ T_2\ z$
T_0	0 0	0	0 0	1 0 0 0
T_0	0 0	1	0 1	1 0 0 0
T_1	0 1	0	1 1	0 1 0 0
T_1	0 1	1	0 1	0 1 0 0
T_2	1 1	0	0 0	0 0 1 0
T_2	1 1	1	0 1	0 0 1 1

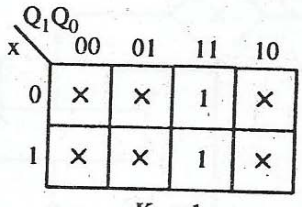
Table below show the excitation table of the flip-flop inputs

Table 7.4

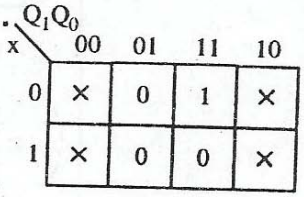
Input x	Present State $Q_1\ Q_0$	Next State $Q_1\ Q_0$	Flip-flop inputs $J_1\ K_1\ J_0\ K_0$
0	0 0	0 0	0 × 0 ×
1	0 0	0 1	0 × 1 ×
0	0 1	1 1	1 × × 0
1	0 1	0 1	0 × × 0
0	1 1	0 0	× 1 × 1
1	1 1	0 1	× 1 × 0



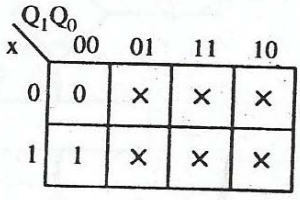
$J_1 = x' Q_0$



$K_1 = 1$

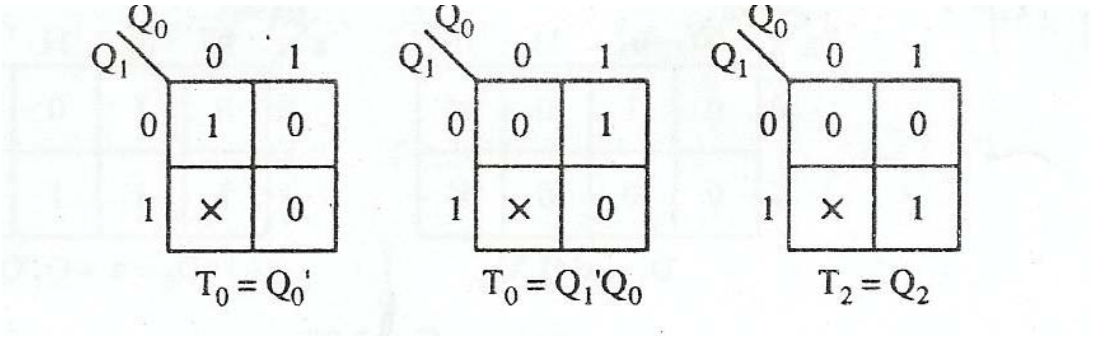


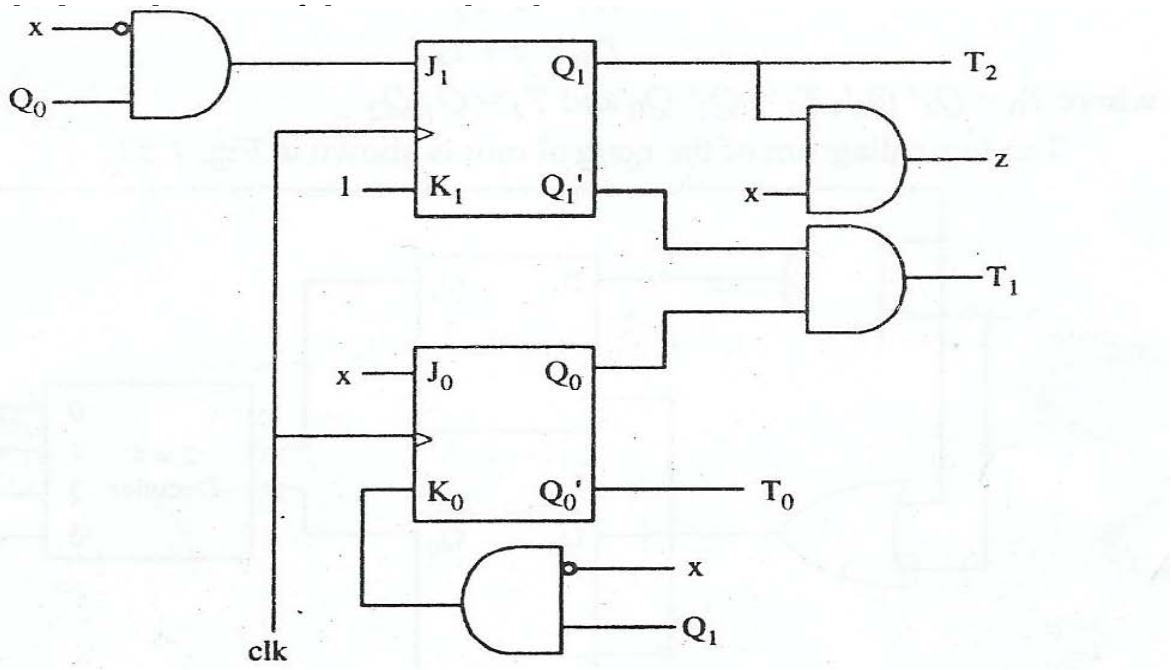
$K_0 = x' Q_1$



$J_0 = x$

Similarty, the three simplified output functions are
To=Q'o
T1=Q'1Qo
T2=Q1





2.Using D flip-flops decoder. The main advantage of this method is that we can directly obtain the input functions from the state table without the need of an excitation table .This is because the next state is the same as the input requirement for D flip-flops. Then instead of using the flip-flop output as the present state condition ,we might as well use the output of the decoder to supply this information ,for that insert a decoder at the output of the flip flops to obtain the necessary output

Example

Design the control unit whose state table is given in Table below using logic gates ,D flip-flops and decoder.

x \ Q_1Q_0	00	01	11	10
0	0	1	0	×
1	0	0	0	×

$D_1 = x' Q_1' Q_0$

x \ Q_1Q_0	00	01	11	10
0	0	1	0	×
1	1	1	1	×

$D_0 = x + Q_1' Q_0$

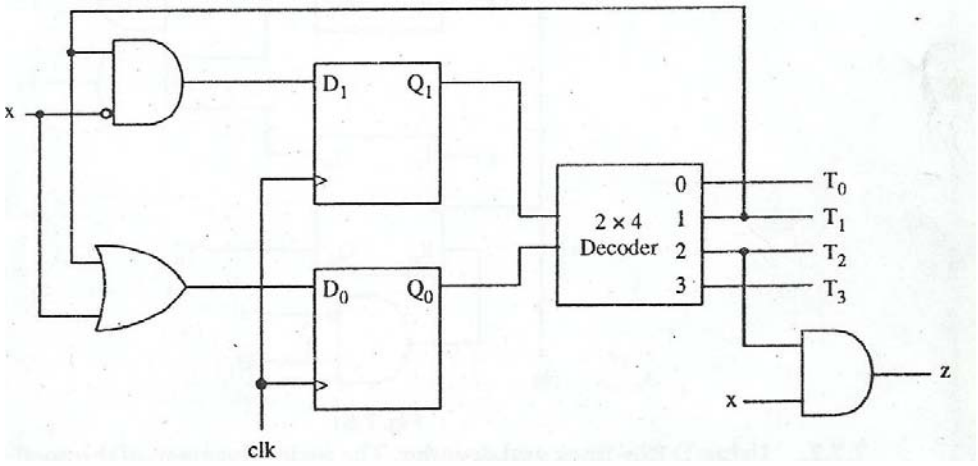
The input functions to the *D* flip-flops can also be expressed as follows :

$$D_1 = x' T_1$$

$$D_0 = x + T_1.$$

re $T_0 = Q_1' Q_0'$, $T_1 = Q_1' Q_0$ and $T_2 = Q_1 Q_2$

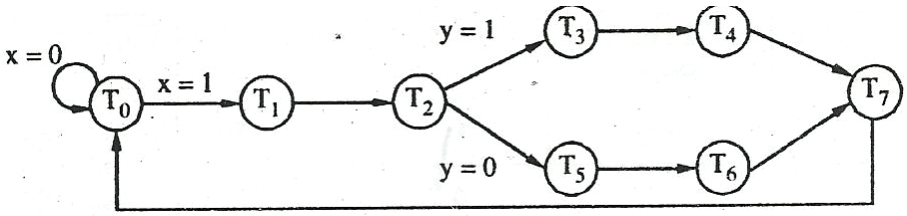
The logic diagram of the control unit is shown in Fig. below



3.Using one flip flop per state This method uses one flip-flop per state in the control sequential circuit .Each flip-flop is set at any particular time , while all others are clear .The advantage of this method is simplicity with which it cant designed .The control unit logic can be derived directly from the state diagram without the need of state or excitation tables .The main disadvantage of this method is that it uses a maximums number of flip-flops.

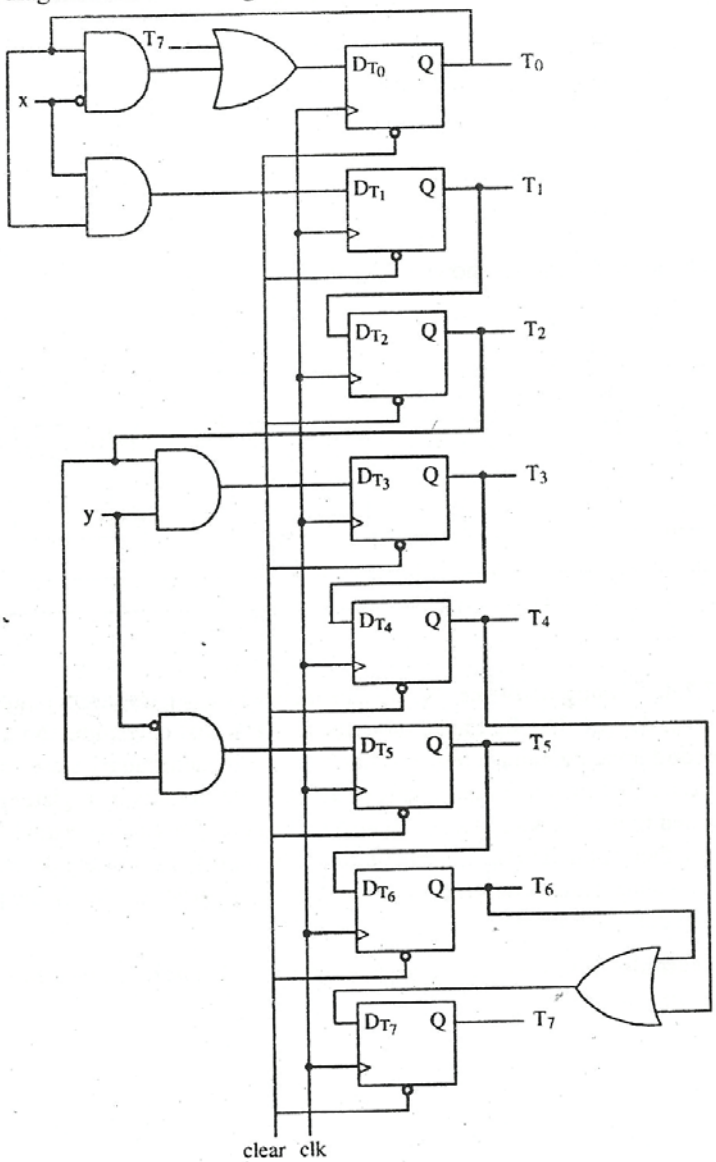
Example

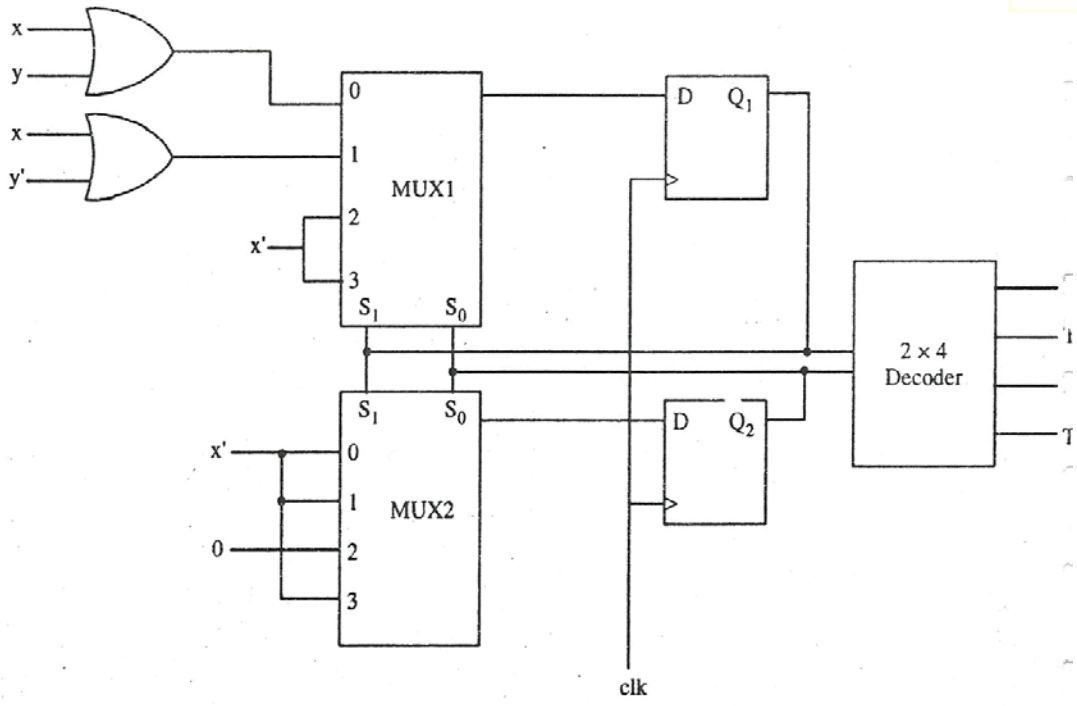
A control unit has two inputs x and y and eight states .The control state diagram is shown in Fig. below .Design the control using eight D flip-flops.



$D_{T_0} = x'T_0 + T_7$
$D_{T_1} = x\,T_0$
$D_{T_2} = T_1$
$D_{T_3} = yT_2$
$D_{T_4} = T_3$
$D_{T_5} = y'T_2$
$D_{T_6} = T_5$
$D_{T_7} = T_4 + T_6.$

The logic diagram is shown in Fig. 7.55.




x
y
x
y'
0
1
2
3
MUX1
x'
S1
S0
D
Q1
2 × 4
Decoder
S1
S0
x'
0
1
MUX2
0
2
3
D
Q2
clk